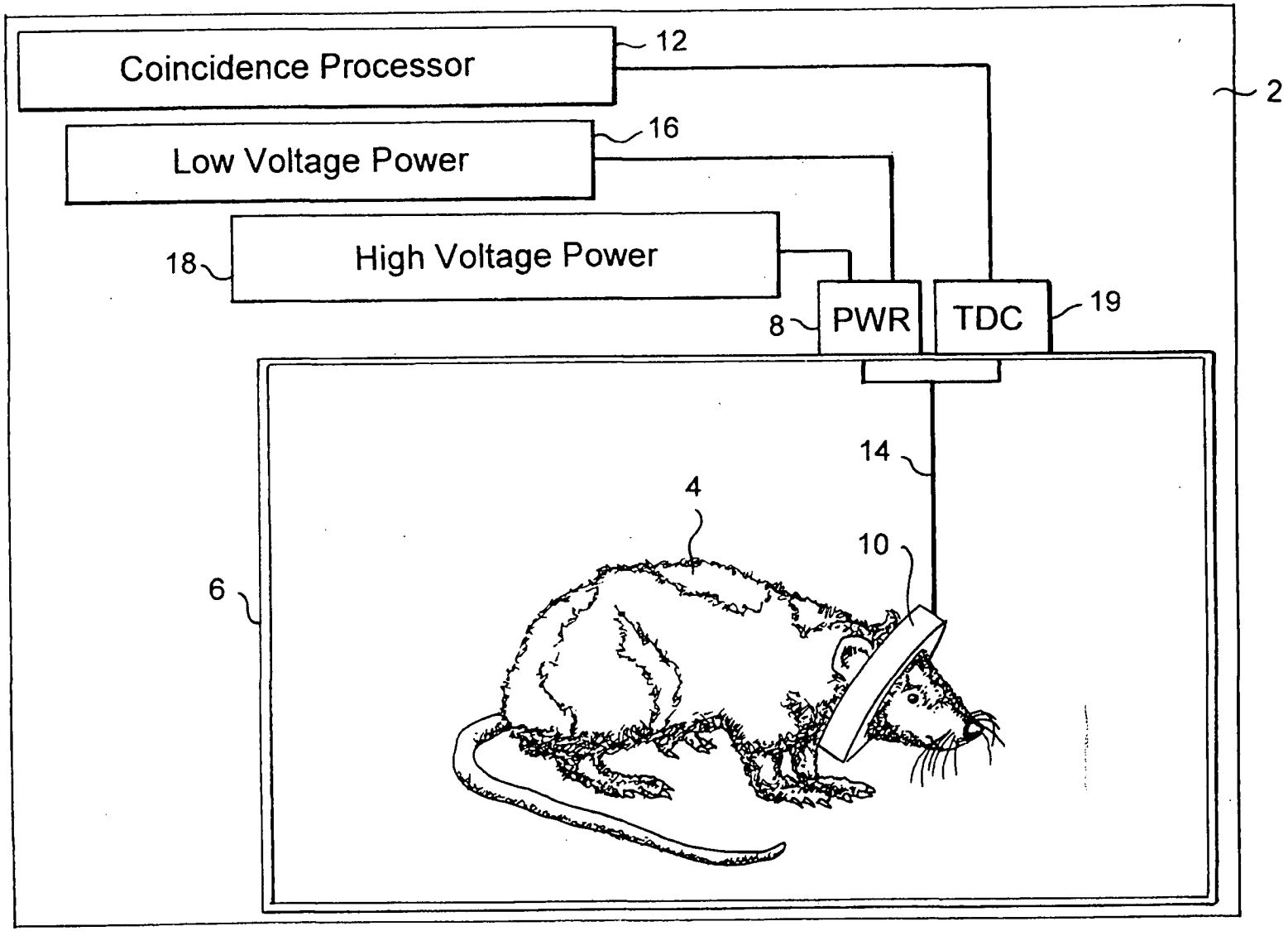



Figure 1

PATENT & TRADEMARK OFFICE
SEP 20 2004
OIPE

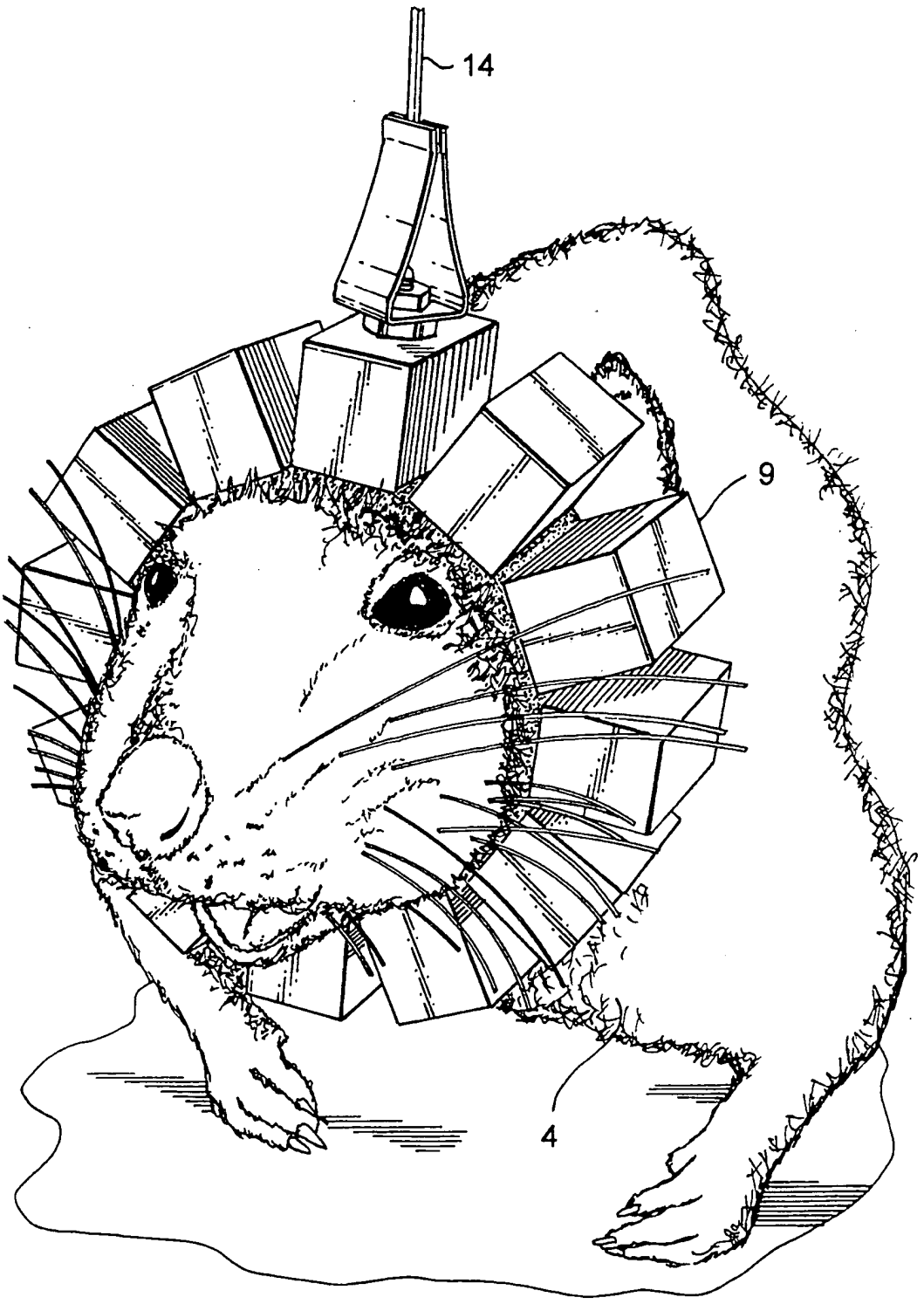



Figure 2

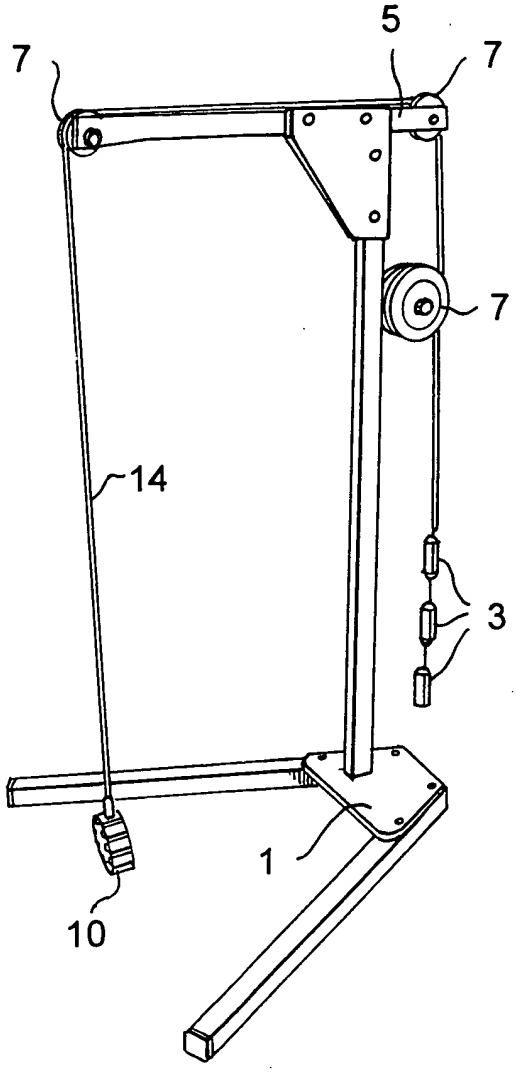



Figure 3a

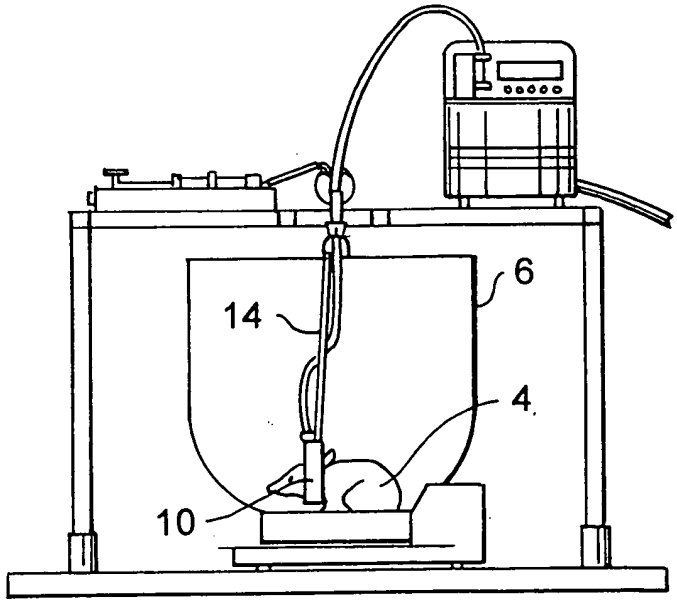



Figure 3b

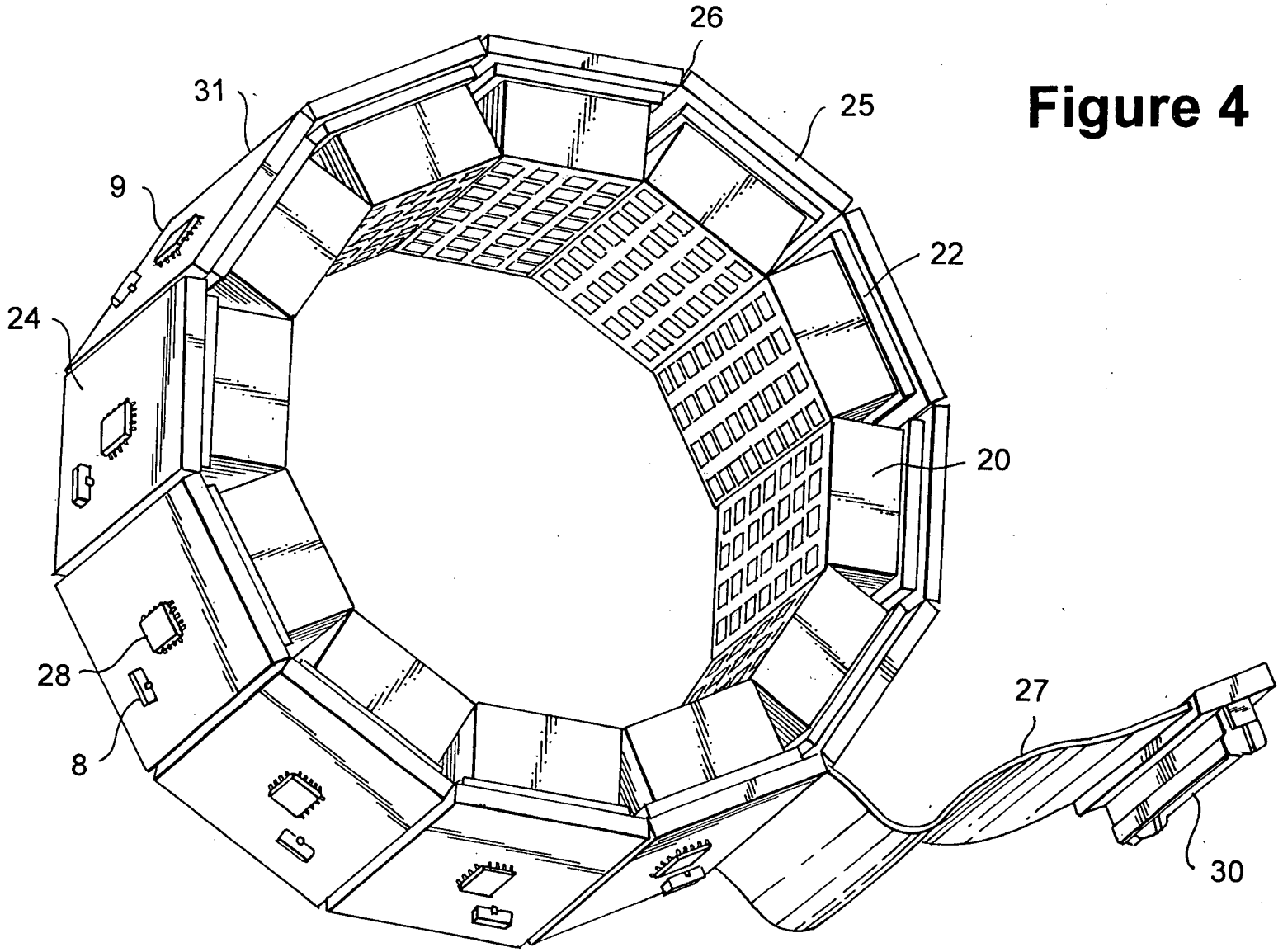



**Figure 4**

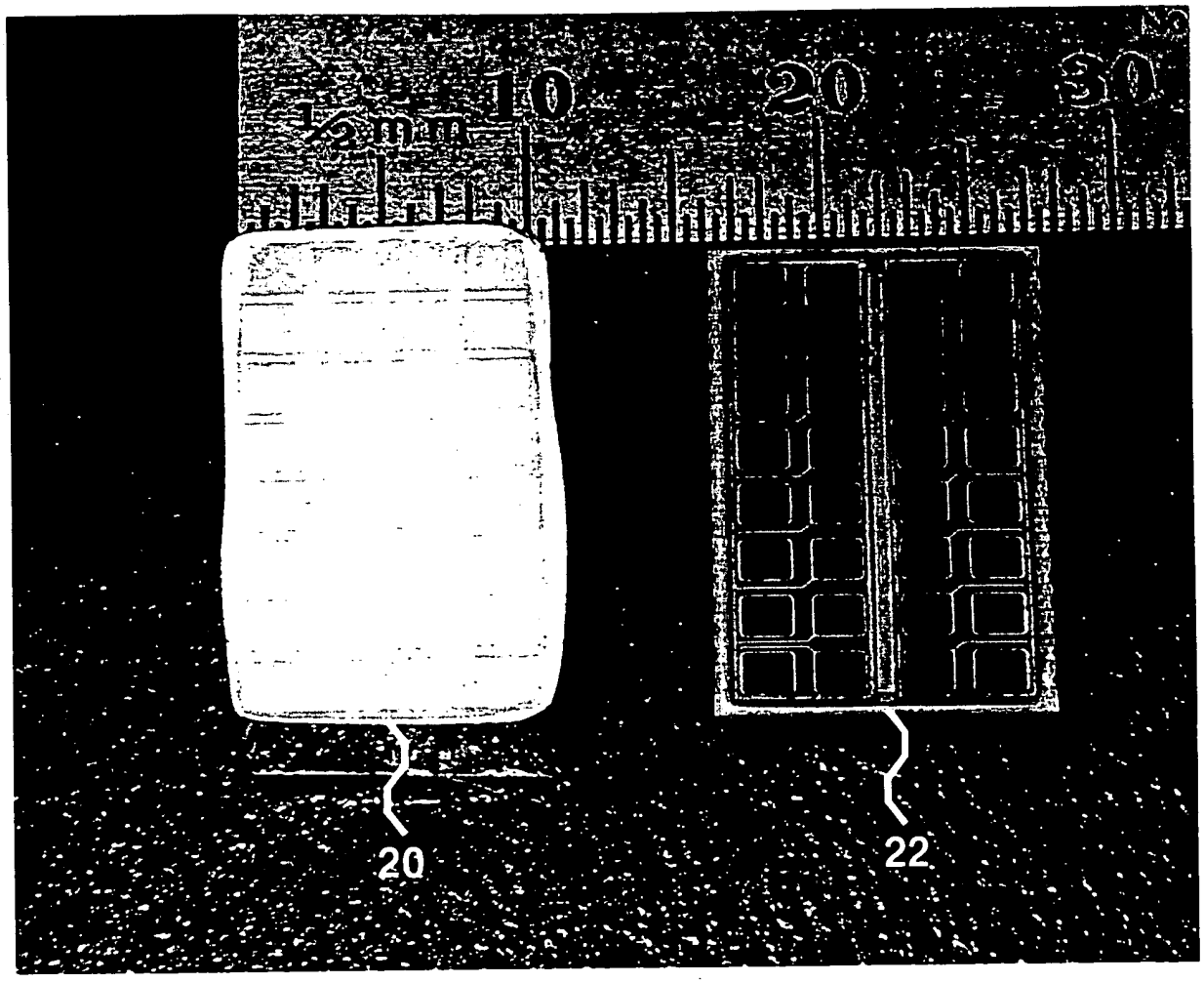



**Figure 5**

BEST AVAILABLE COPY

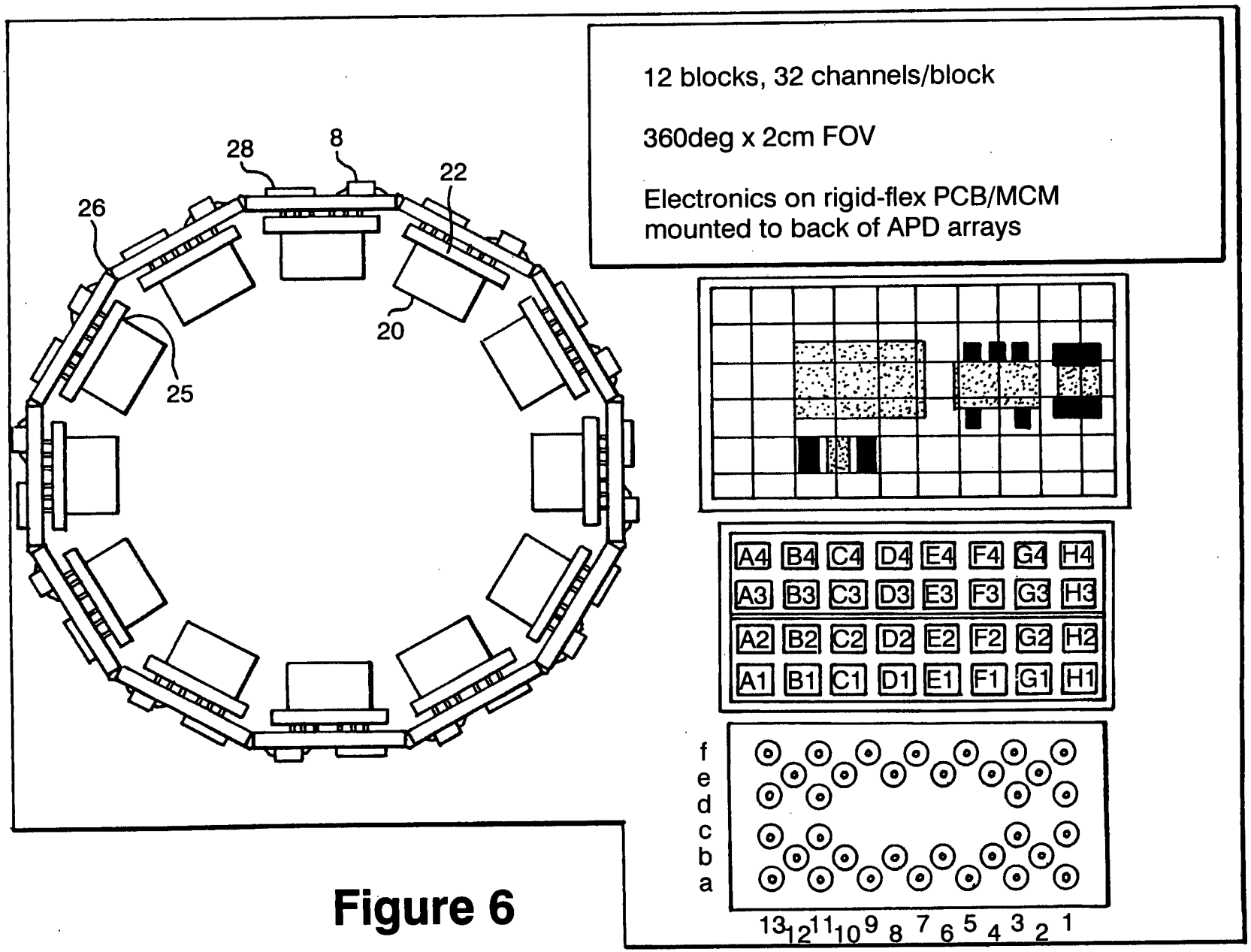
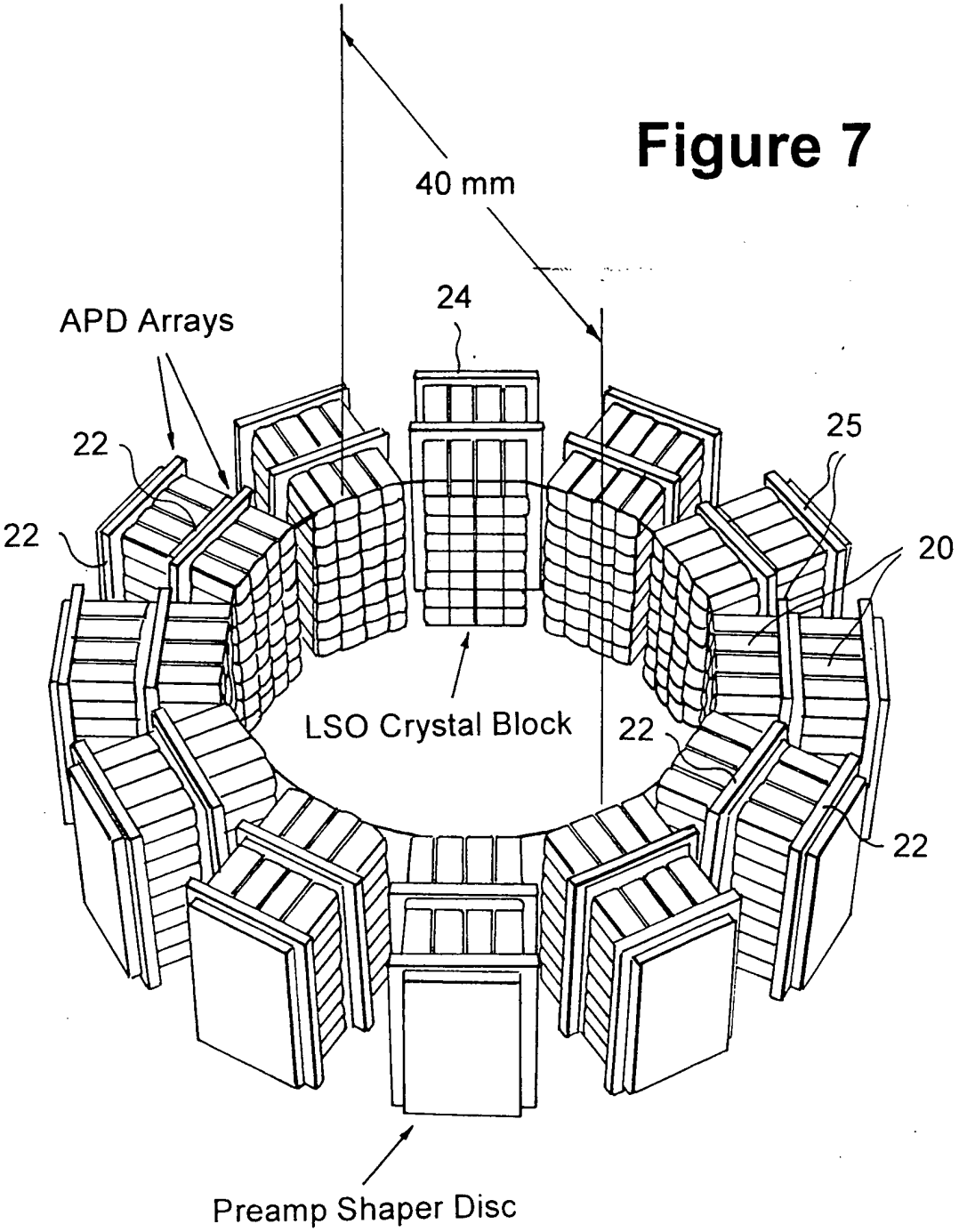

12 blocks, 32 channels/block
360deg x 2cm FOV
Electronics on rigid-flex PCB/MCM mounted to back of APD arrays
28
8
22
26
20
25
A4 B4 C4 D4 E4 F4 G4 H4
A3 B3 C3 D3 E3 F3 G3 H3
A2 B2 C2 D2 E2 F2 G2 H2
A1 B1 C1 D1 E1 F1 G1 H1
f
e
d
c
b
a
13 12 11 10 9 8 7 6 5 4 3 2 1

**Figure 6**

# Figure 7


40 mm
24
APD Arrays
22
22
25
20
LSO Crystal Block
22
22
Preamp Shaper Disc

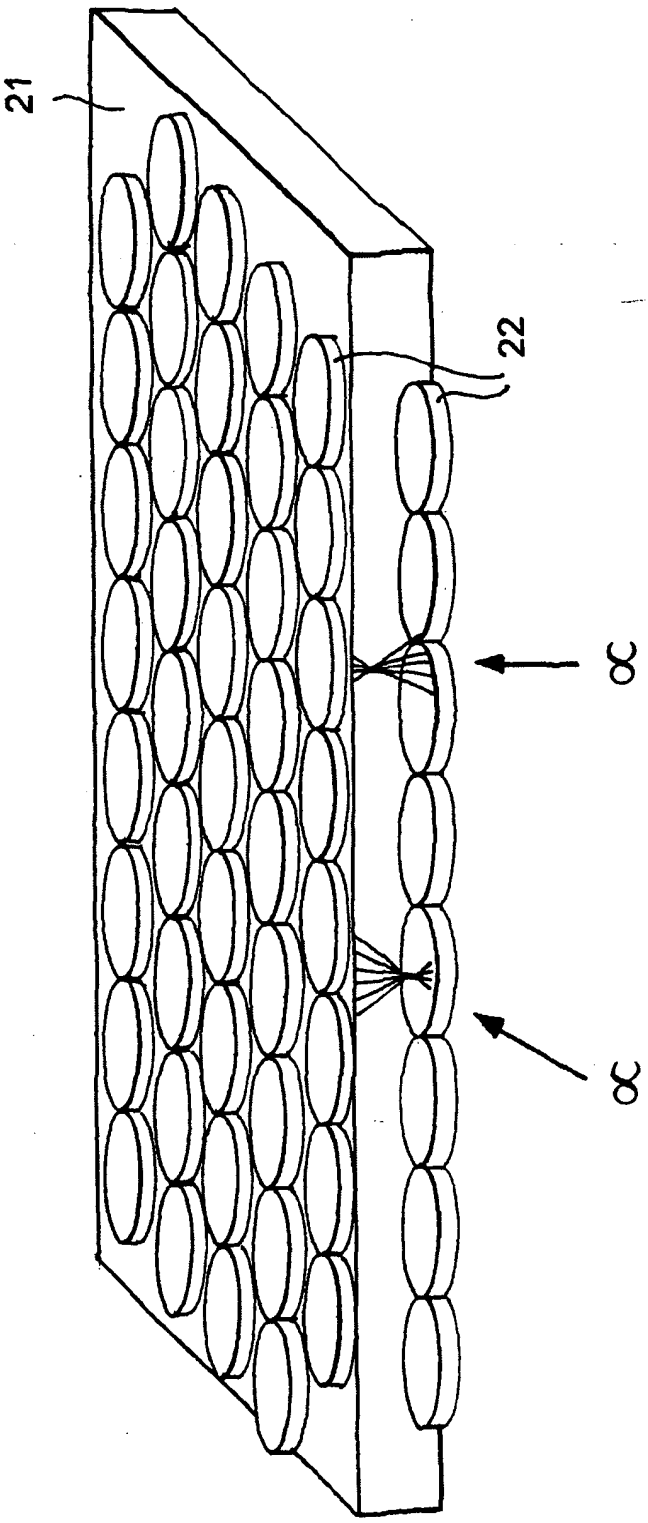



Figure 8

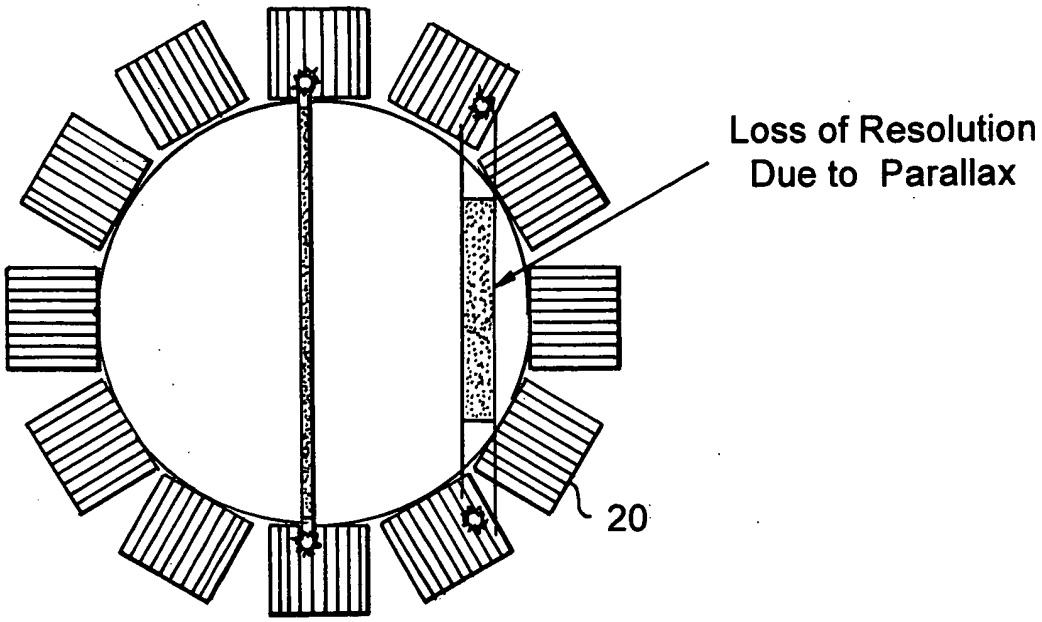



Figure 9a

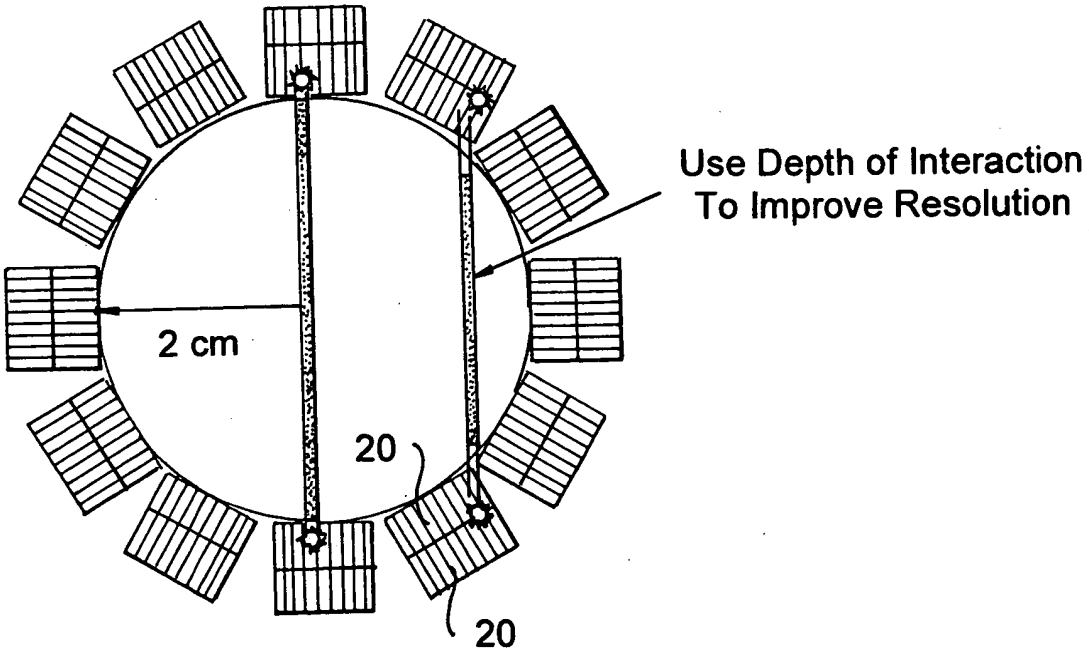
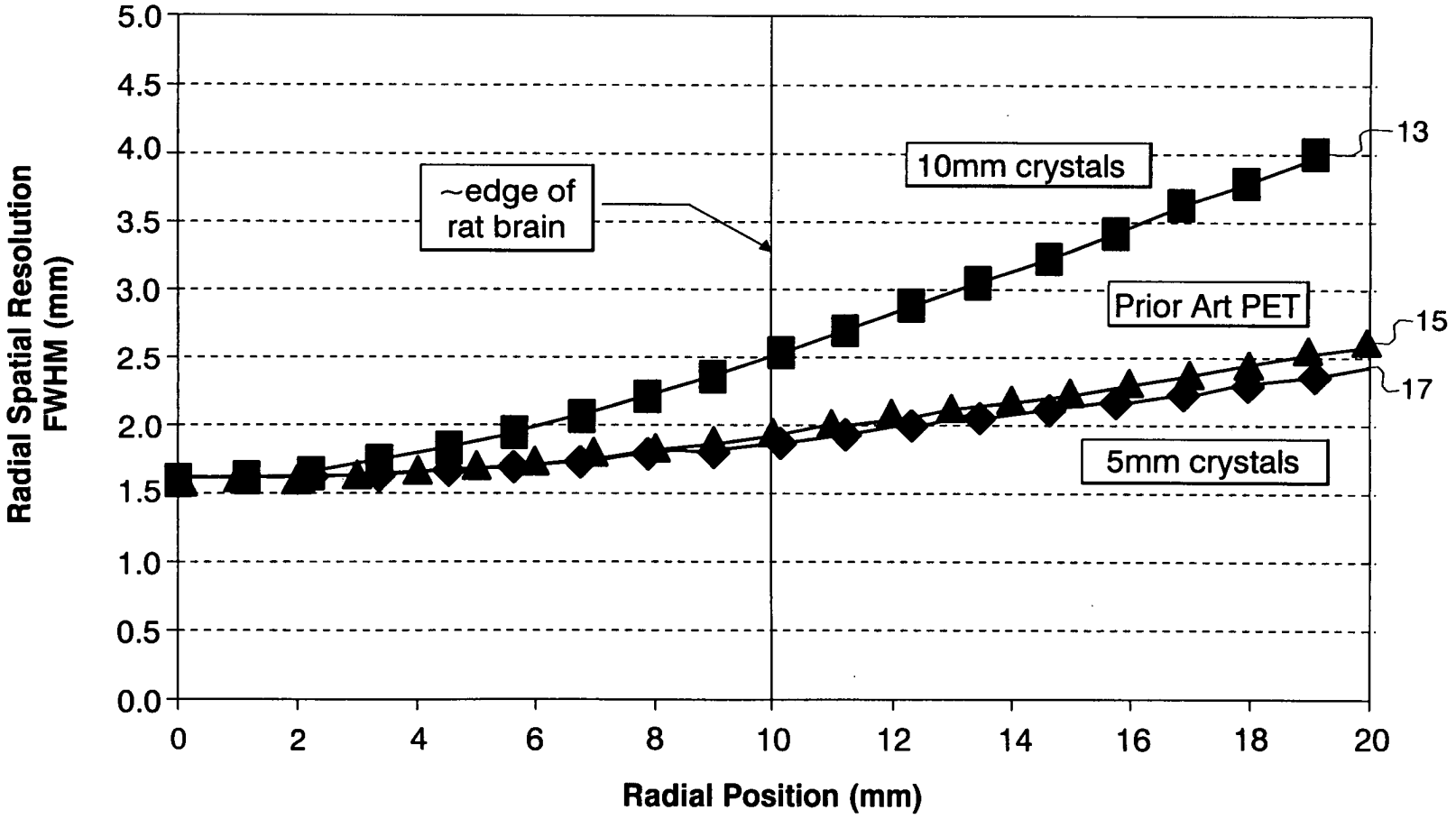



Figure 9b




**Calculated Image Spatial Resolution of BNL nanoPET**

# Figure 10

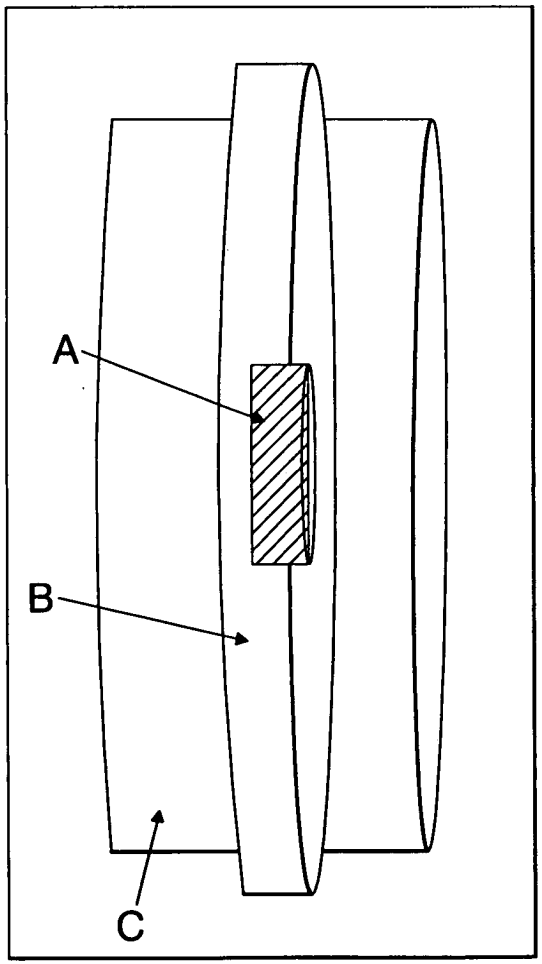



Figure 11a

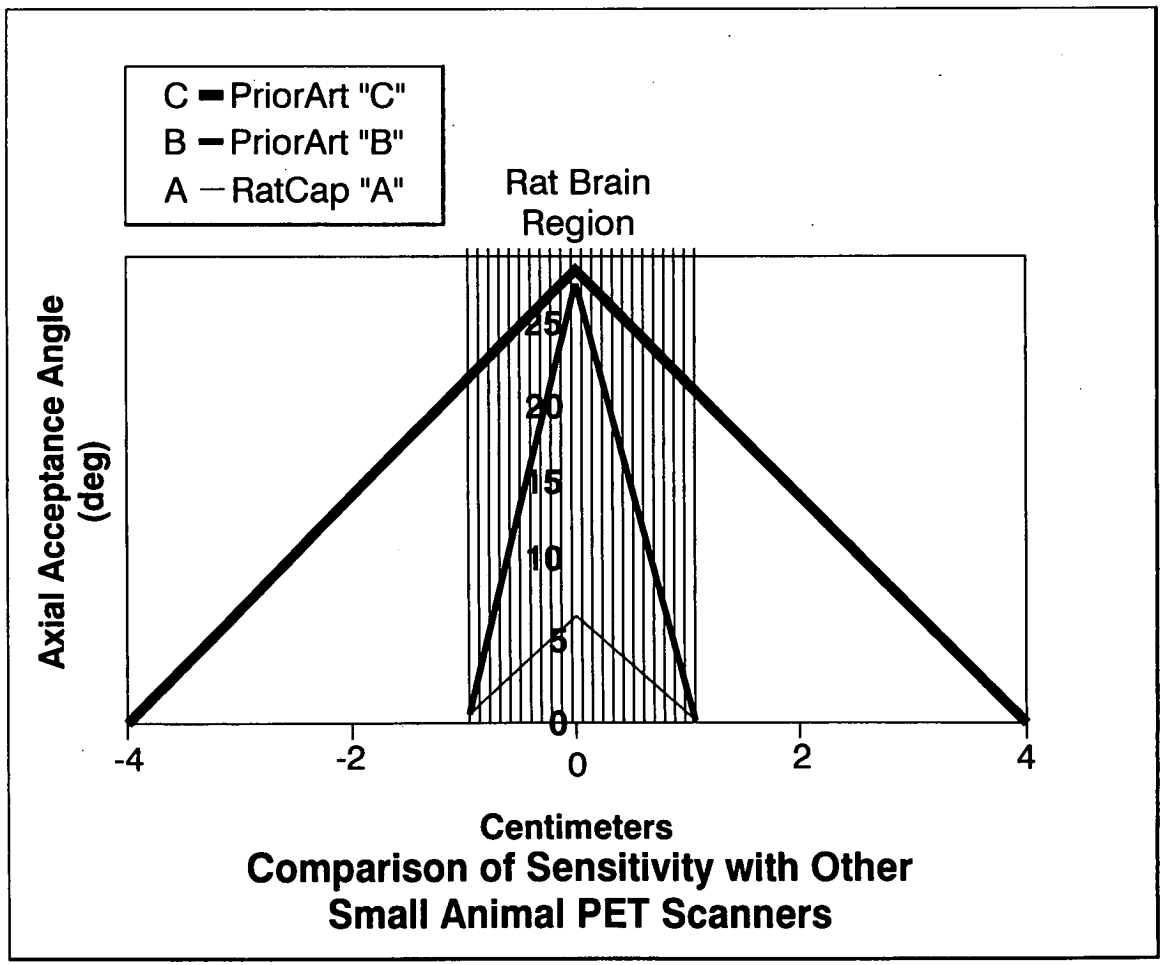



Figure 11b

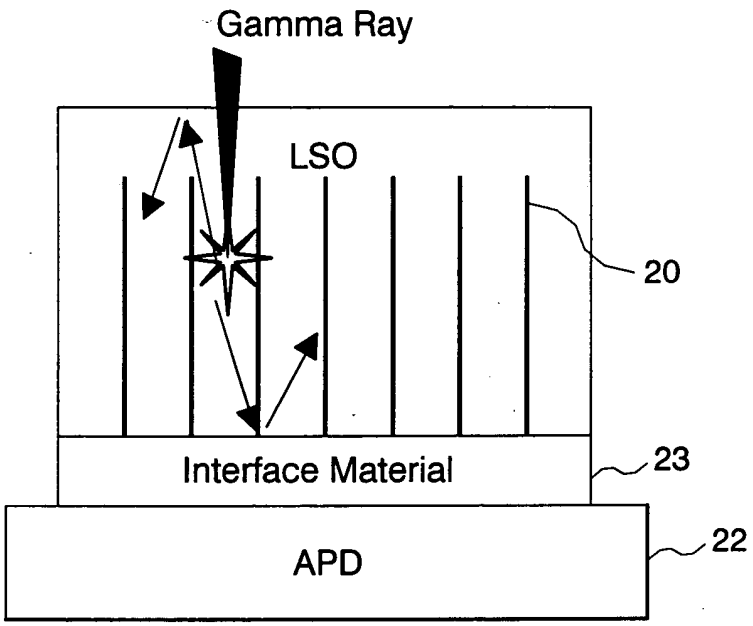



Figure 12a

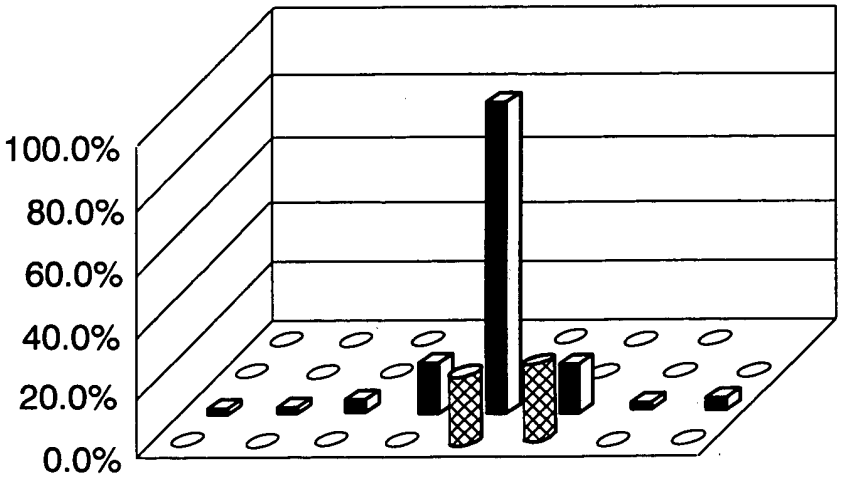
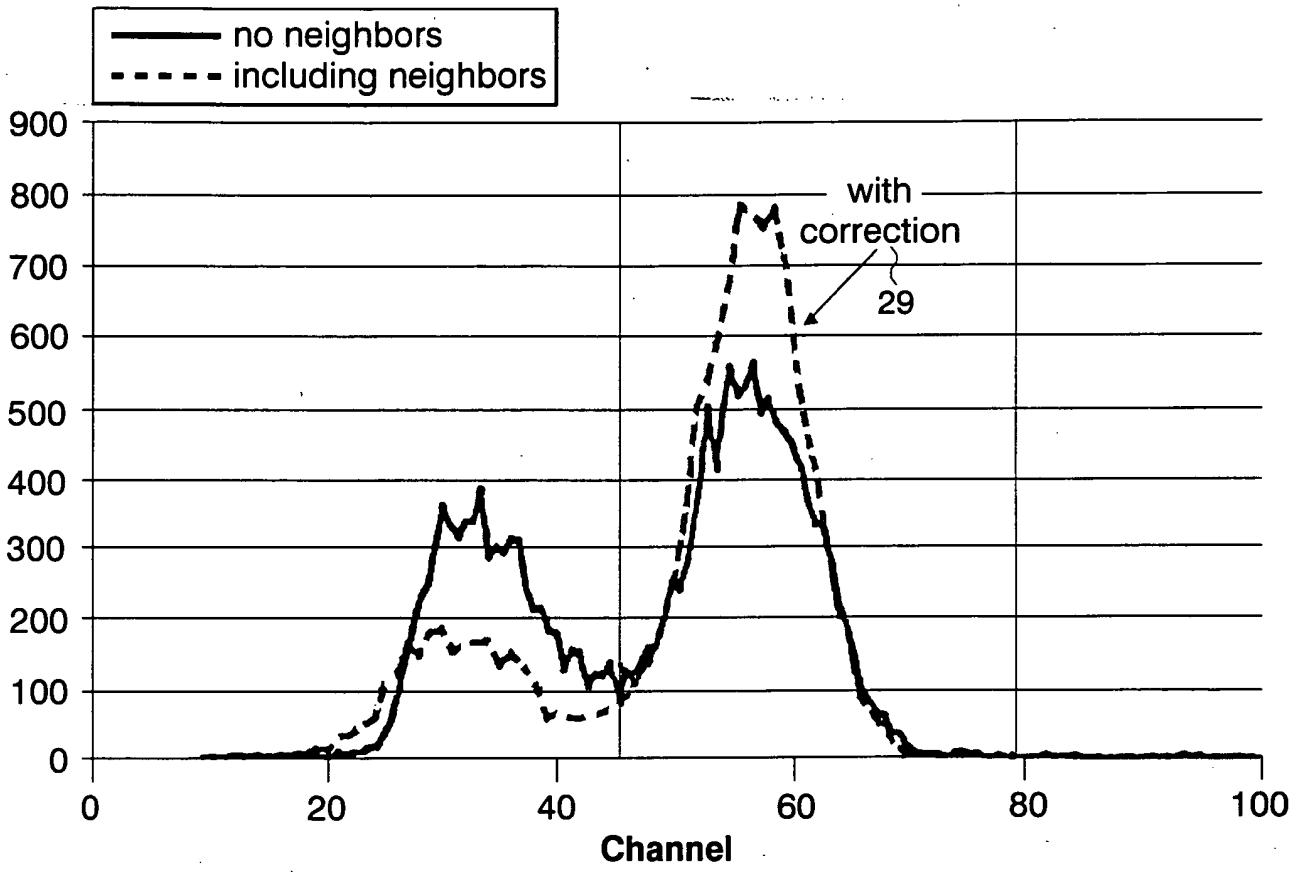



Figure 12b




**Energy Spectra for Crystal 20**

# Figure 12c

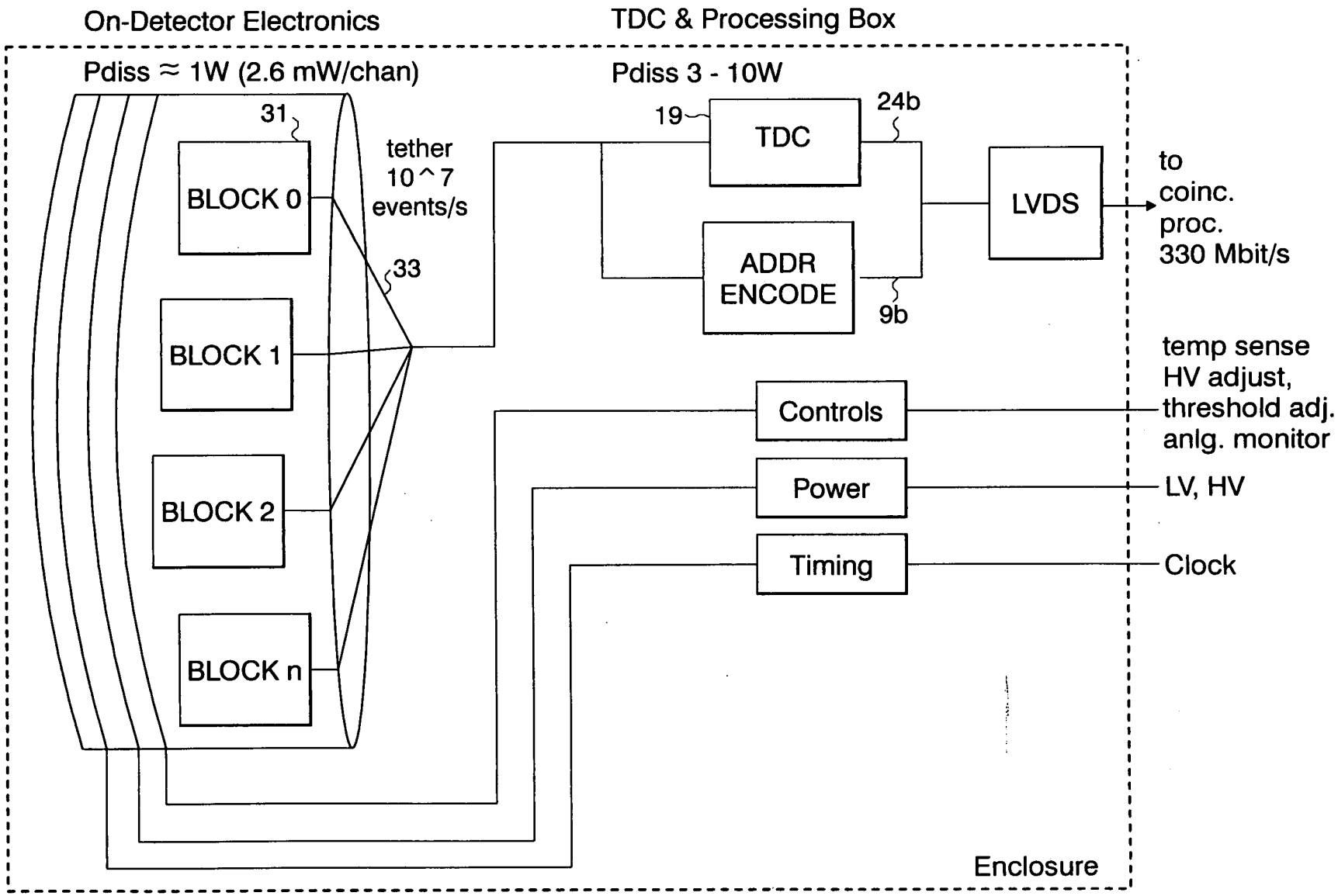
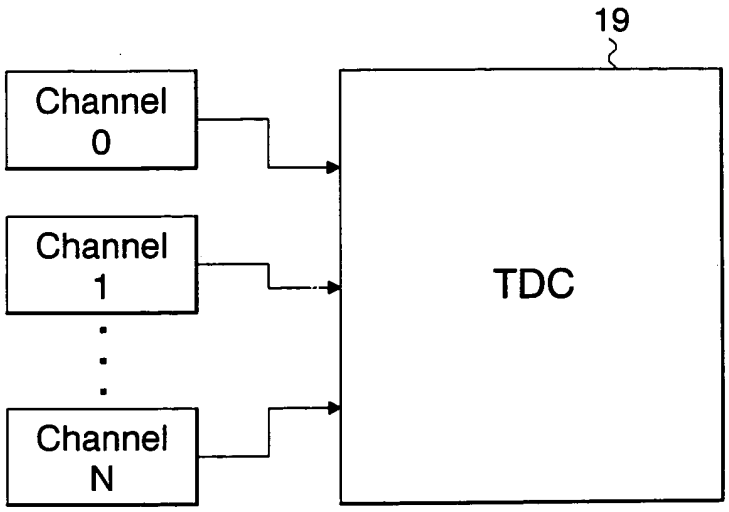

On-Detector Electronics
TDC & Processing Box
Pdiss ≈ 1W (2.6 mW/chan)
Pdiss 3 - 10W
31
BLOCK 0
BLOCK 1
BLOCK 2
BLOCK n
tether
10^7
events/s
33
19
TDC
24b
ADDR
ENCODE
9b
LVDS
to
coinc.
proc.
330 Mbit/s
Controls
Power
Timing
temp sense
HV adjust,
threshold adj.
anlg. monitor
LV, HV
Clock
Enclosure

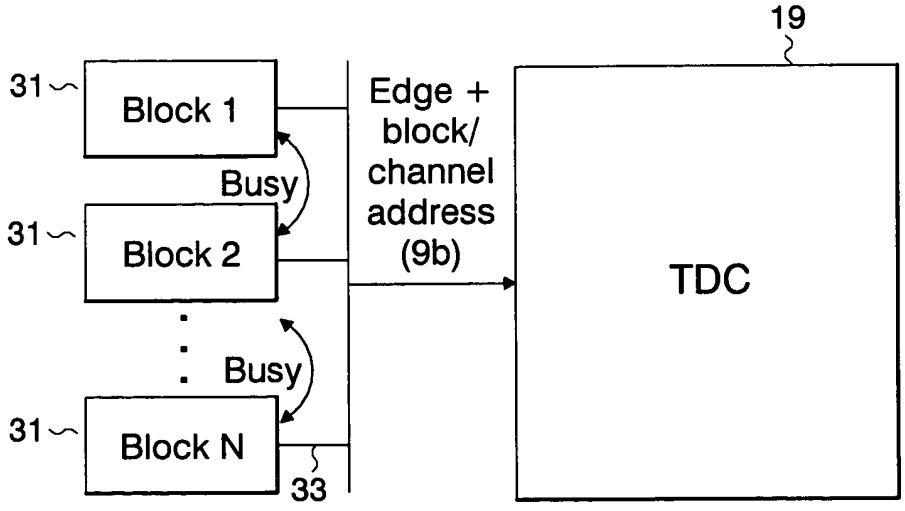
**Figure 13**




**Individual Serial Links**

# Figure 14a

***(Prior Art)***




**Common Serial Bus with Busy**

# Figure 14b

**Serial Link Timing**

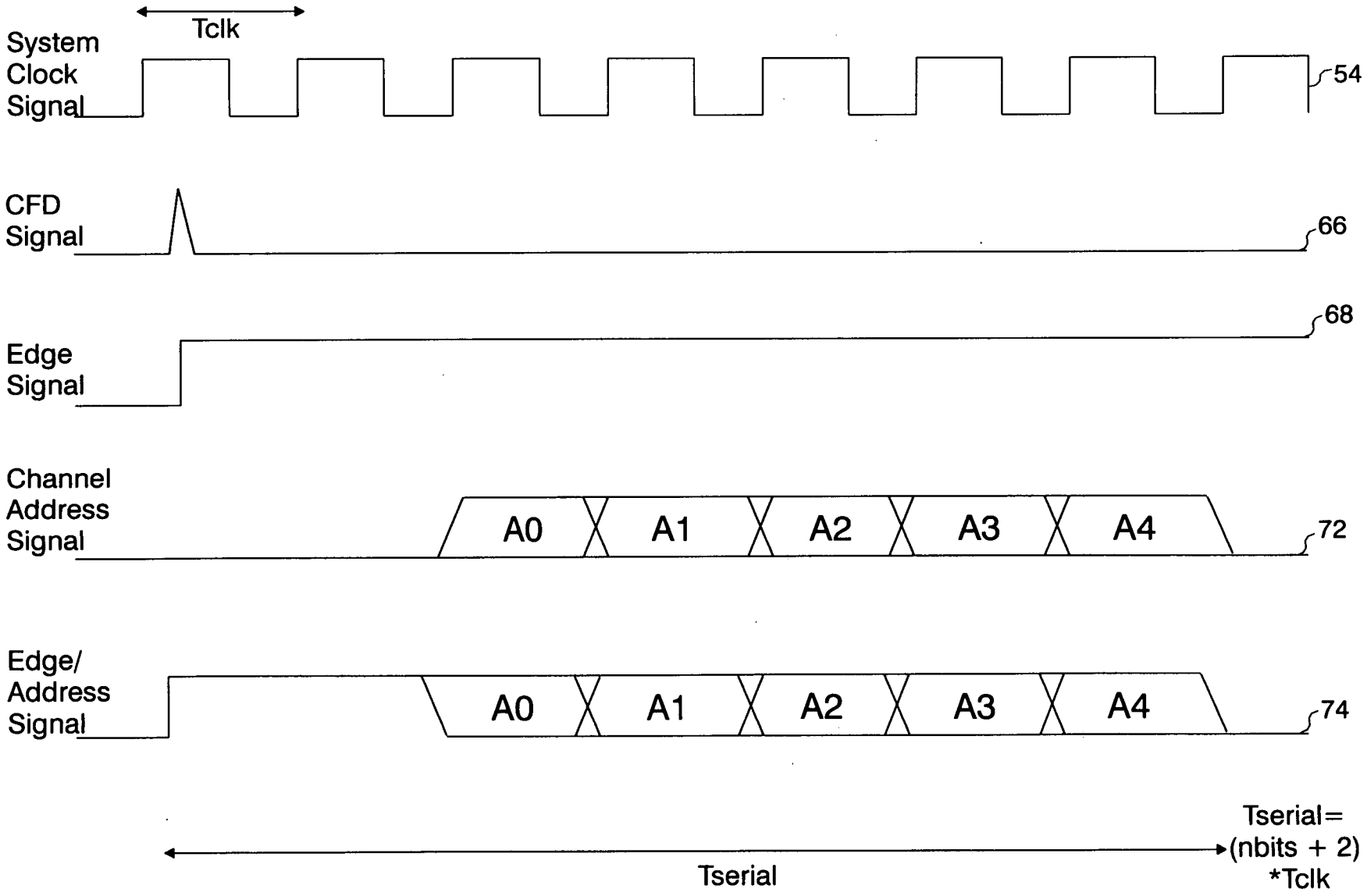



**Figure 15**

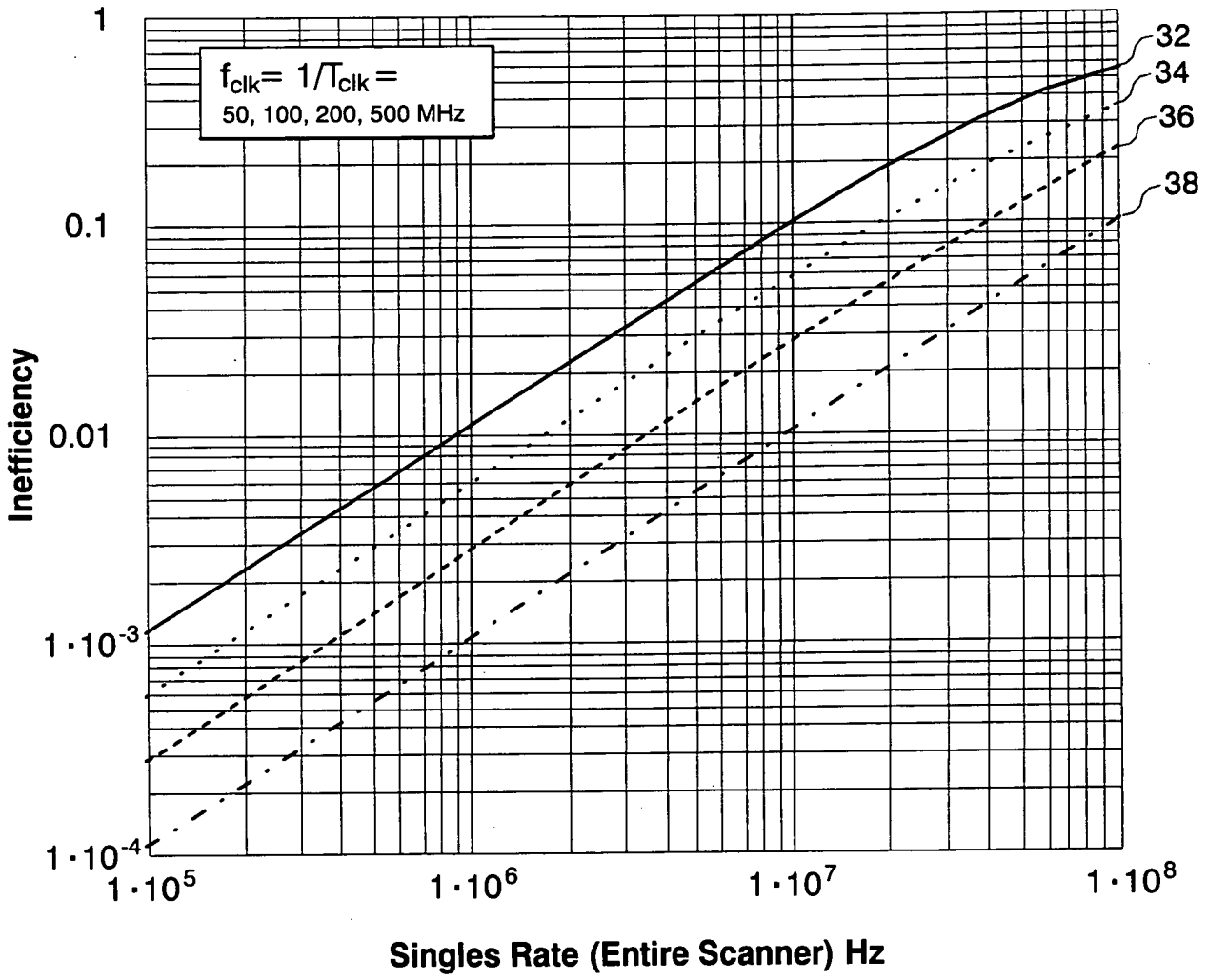

1
0.1
0.01
1·10-3
1·10-4
Inefficiency
fclk= 1/Tclk =
50, 100, 200, 500 MHz
32
34
36
38
1·105
1·106
1·107
1·108
Singles Rate (Entire Scanner) Hz

**Figure 16**

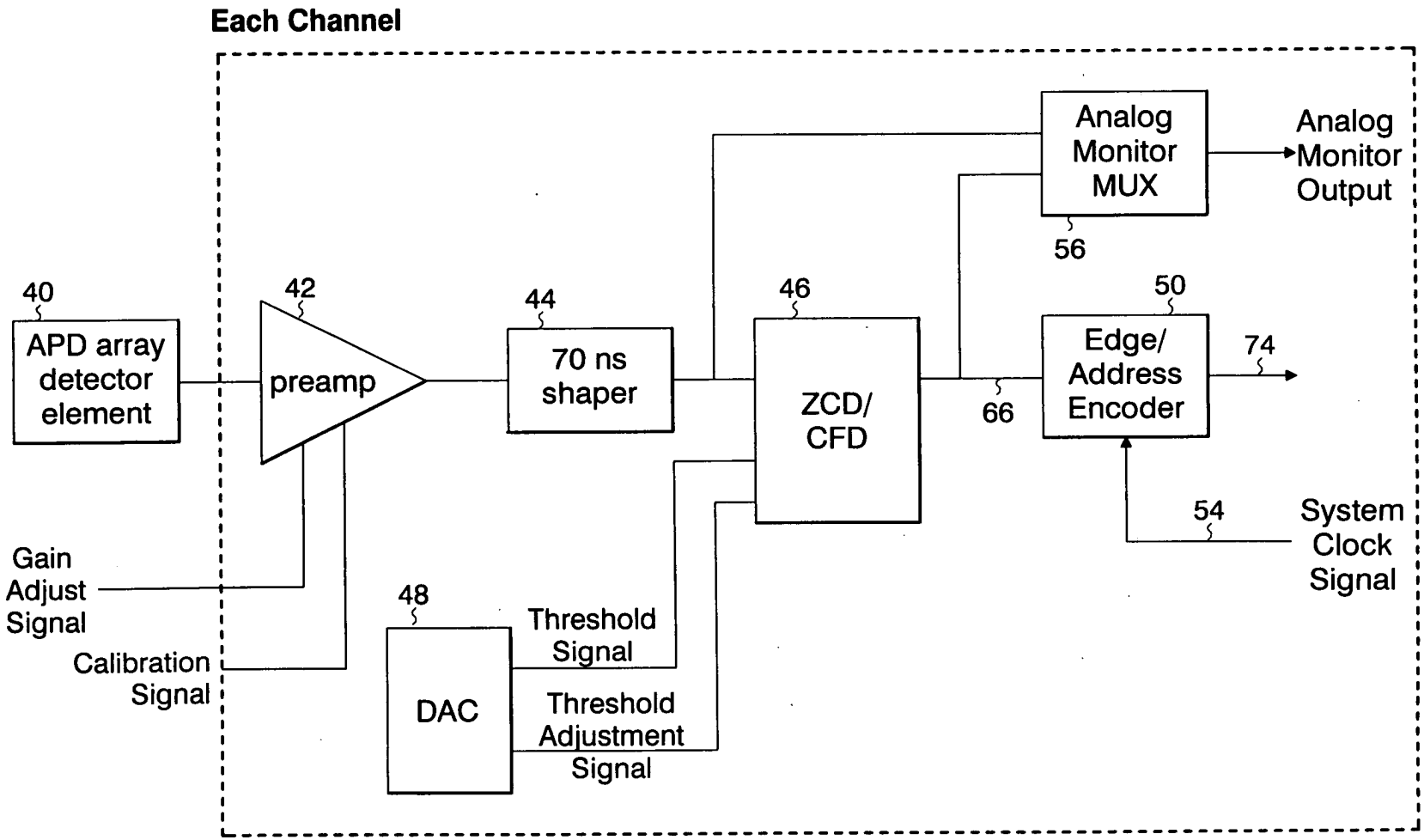

Each Channel
Analog Monitor MUX
Analog Monitor Output
56
40
APD array detector element
42
preamp
44
70 ns shaper
46
ZCD/ CFD
50
Edge/ Address Encoder
74
66
54
System Clock Signal
Gain Adjust Signal
Calibration Signal
48
DAC
Threshold Signal
Threshold Adjustment Signal

**Figure 17**

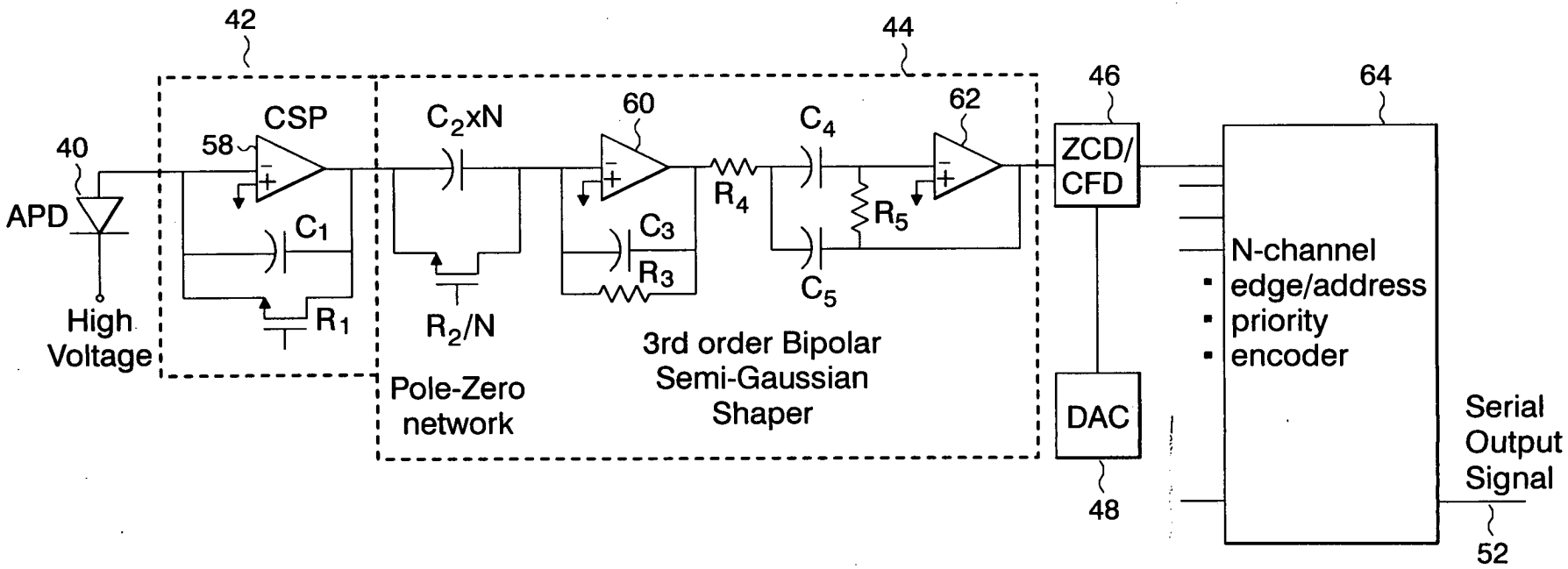

42
44
46
64
CSP
58
40
APD
High
Voltage
C1
R1
C2xN
R2/N
Pole-Zero
network
60
C3
R3
R4
C4
62
R5
C5
3rd order Bipolar
Semi-Gaussian
Shaper
ZCD/
CFD
DAC
48
N-channel
edge/address
priority
encoder
Serial
Output
Signal
52

**Figure 18**

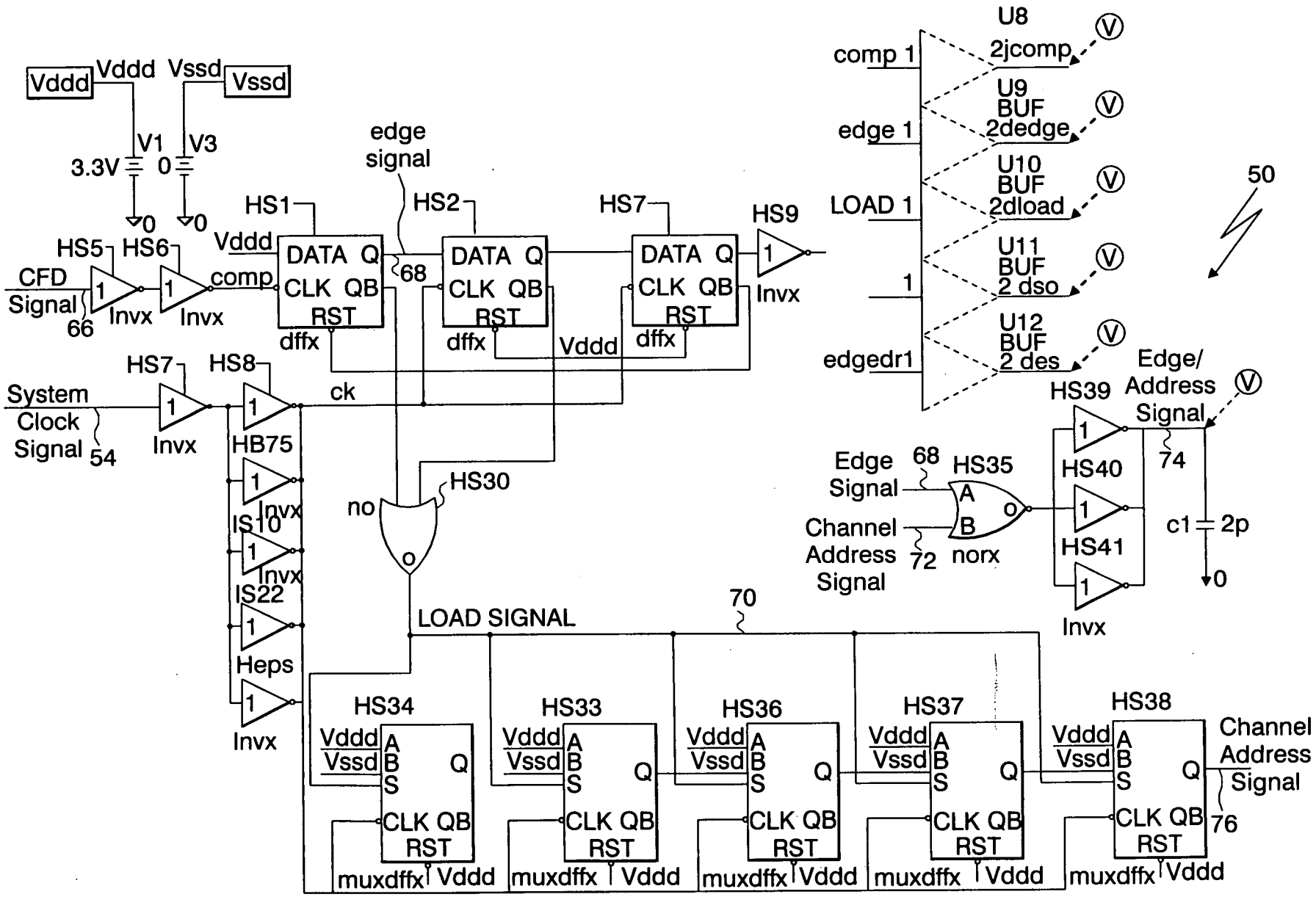

Vddd
Vddd
Vssd
Vssd
V1
V3
3.3V
0
0
0
HS1
HS2
HS7
HS9
edge
signal
HS5
HS6
CFD
Signal
66
Invx
Invx
comp
Vddd
DATA Q
CLK QB
RST
dffx
68
DATA Q
CLK QB
RST
dffx
Vddd
DATA Q
CLK QB
RST
dffx
Invx
U8
2jcomp
comp 1
U9
BUF
2dedge
edge 1
U10
BUF
2dload
LOAD 1
1
U11
BUF
2 dso
U12
BUF
2 des
edgedr1
50
Edge/
Address
Signal
HS7
HS8
System
Clock
Signal
54
Invx
ck
HB75
HS39
HS40
HS41
Invx
74
Edge
Signal
68
HS35
A
B
o
norx
Channel
Address
Signal
72
c1
2p
0
HS10
Invx
HS22
Invx
Heps
Invx
HS30
no
o
LOAD SIGNAL
70
HS34
HS33
HS36
HS37
HS38
Vddd
Vssd
A
B
S
Q
CLK QB
RST
muxdffx
Vddd
Channel
Address
Signal
76

Figure 19

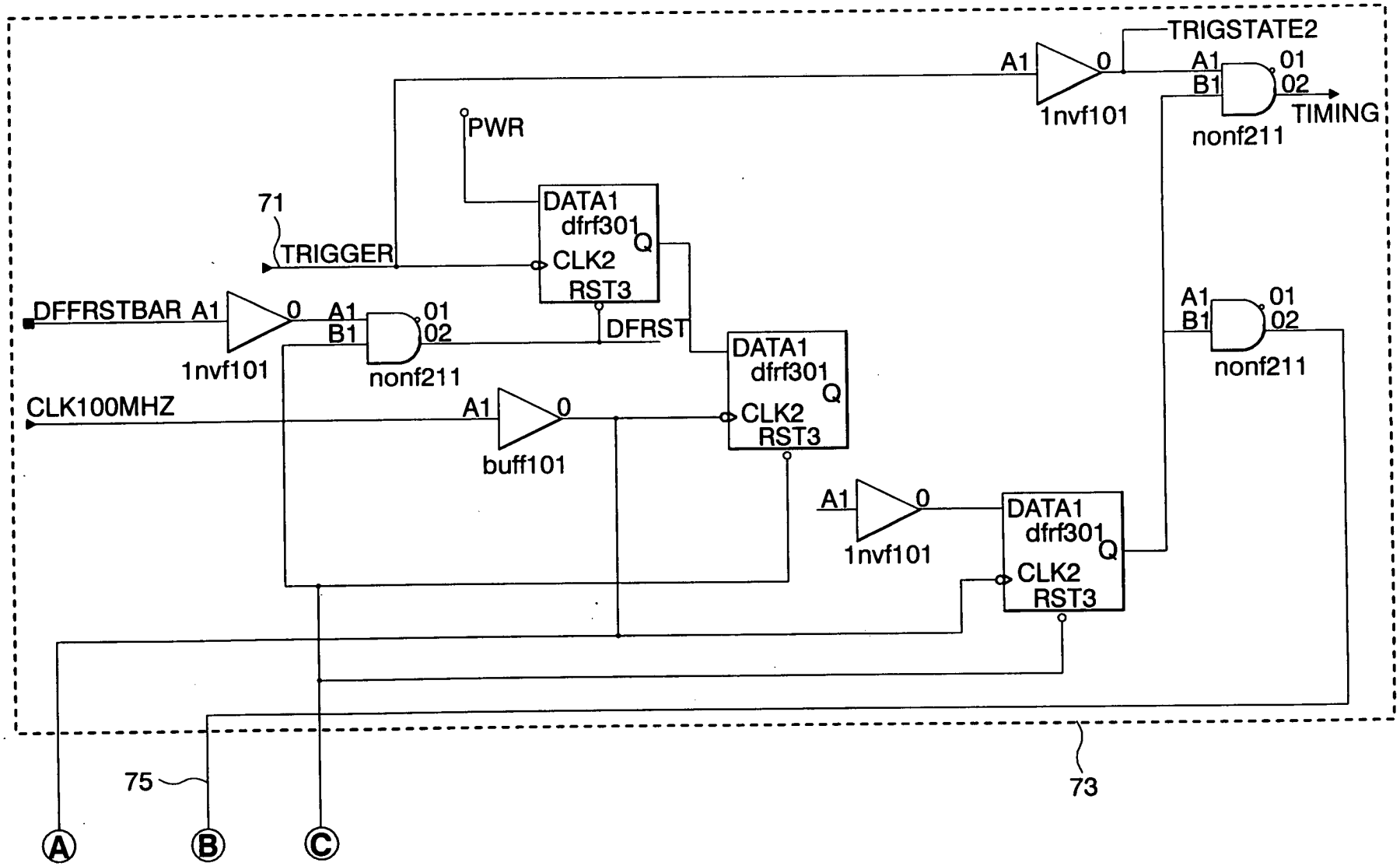
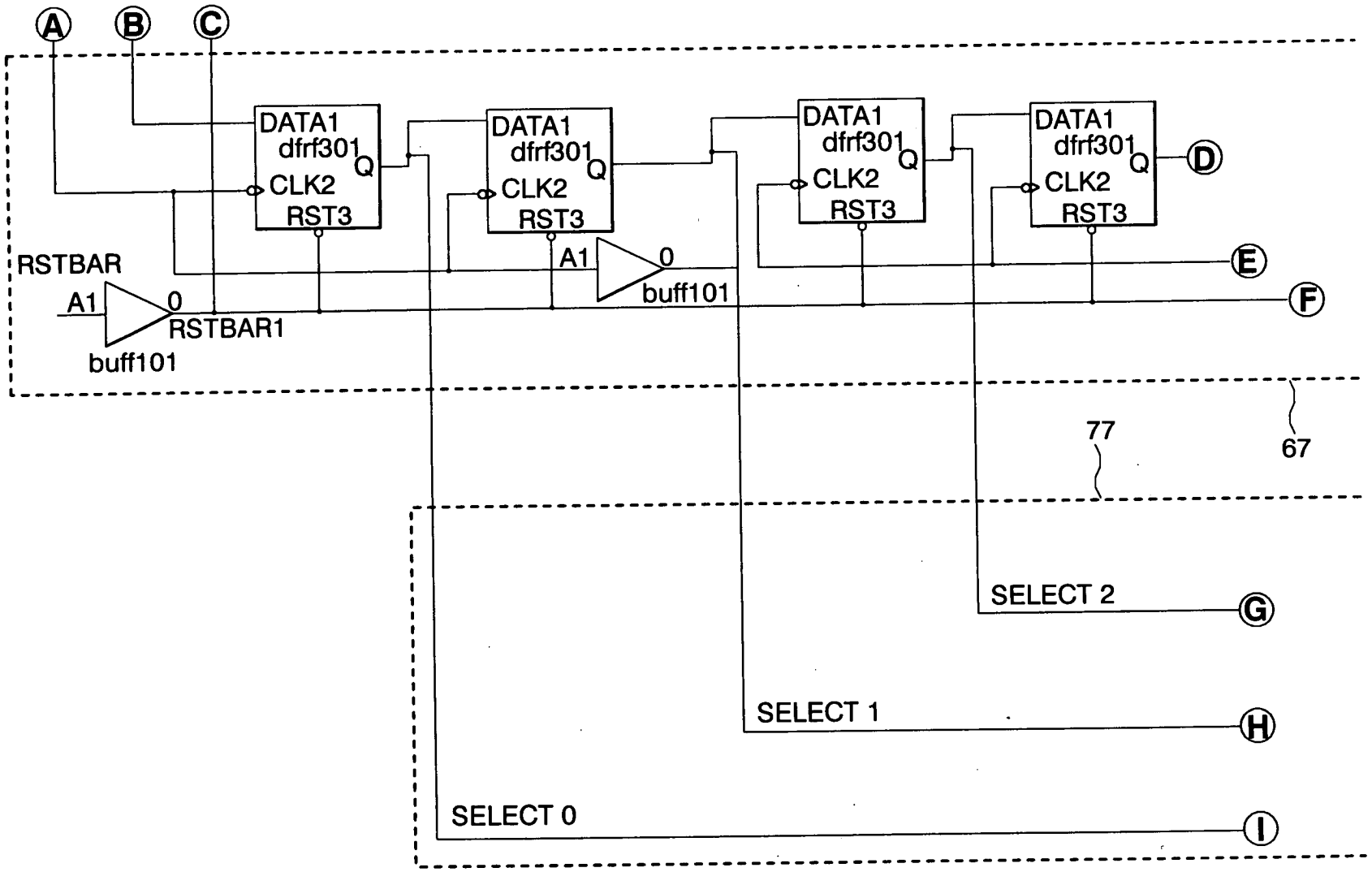

TRIGSTATE2
A1
0
1nvf101
A1
B1
01
02
nonf211
TIMING
PWR
71
TRIGGER
DATA1
dfrf301
Q
CLK2
RST3
DFFRSTBAR
A1
0
1nvf101
A1
B1
01
02
nonf211
DFRST
DATA1
dfrf301
Q
CLK2
RST3
A1
B1
01
02
nonf211
CLK100MHZ
A1
0
buff101
A1
0
1nvf101
DATA1
dfrf301
Q
CLK2
RST3
75
73
A
B
C

Figure 19a(1)




TRIGGER=Asynchronous Trigger
A [4.0]=5 Bit Crystal ID from the 32 to 5 Priority Encoder
SERADD - serialized 5 bit Crystal ID at 100MHz

**Figure 19a(2)**

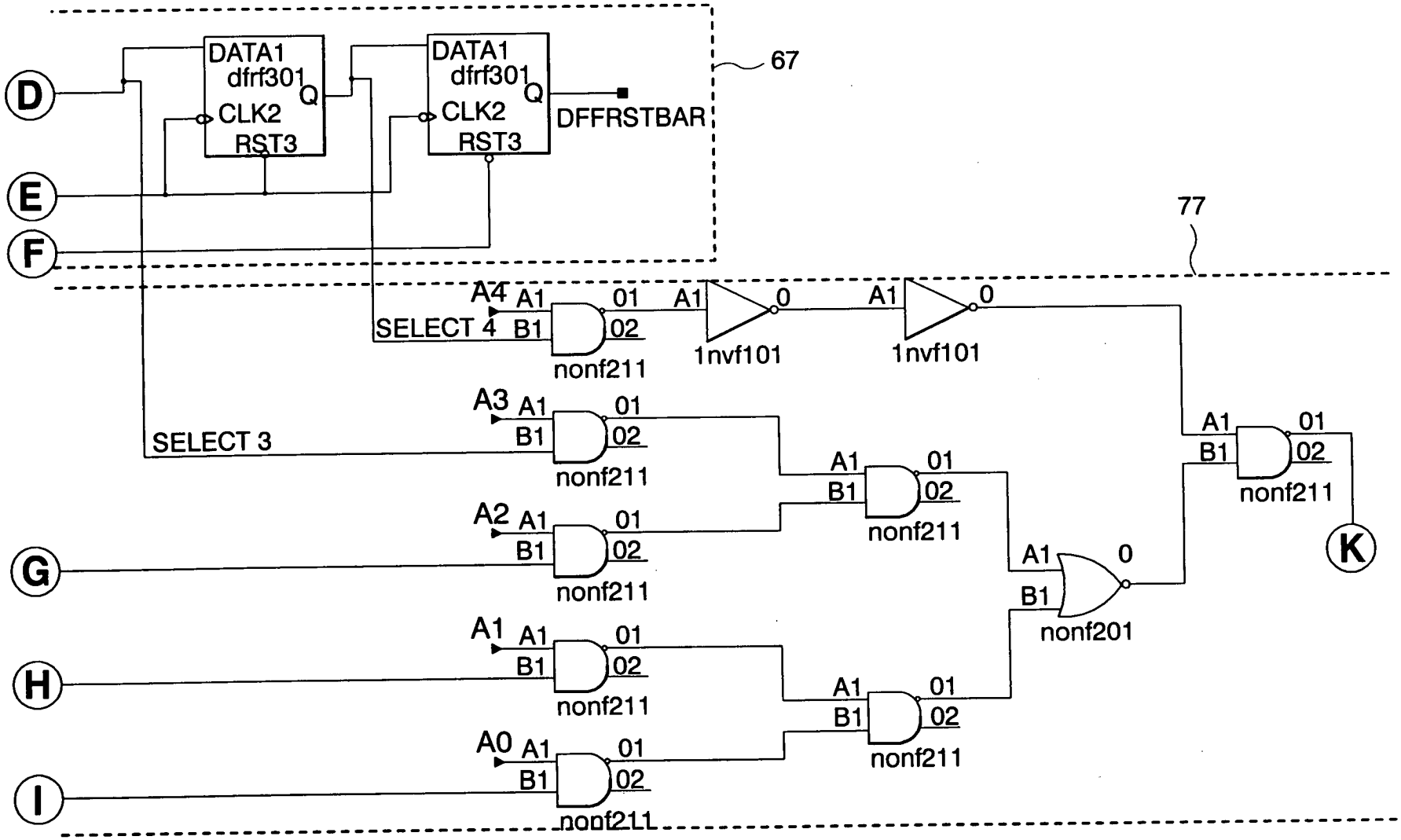

D
E
F
G
H
I
DATA1
dfrf301
Q
CLK2
RST3
DFFRSTBAR
67
77
A4
SELECT 4
A3
SELECT 3
A2
A1
A0
A1
B1
01
02
nonf211
1nvf101
0
nonf201
K

Figure 19a(3)

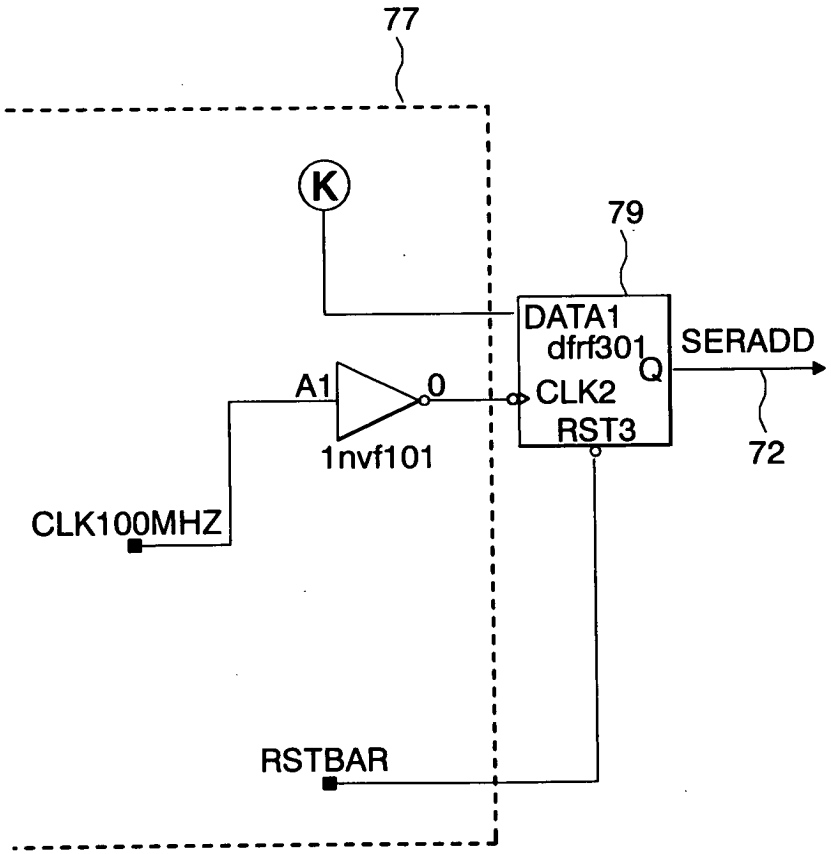

77
K
79
DATA1
dfrf301
Q
SERADD
A1
0
CLK2
RST3
72
1nvf101
CLK100MHZ
RSTBAR

**Figure 19a(4)**

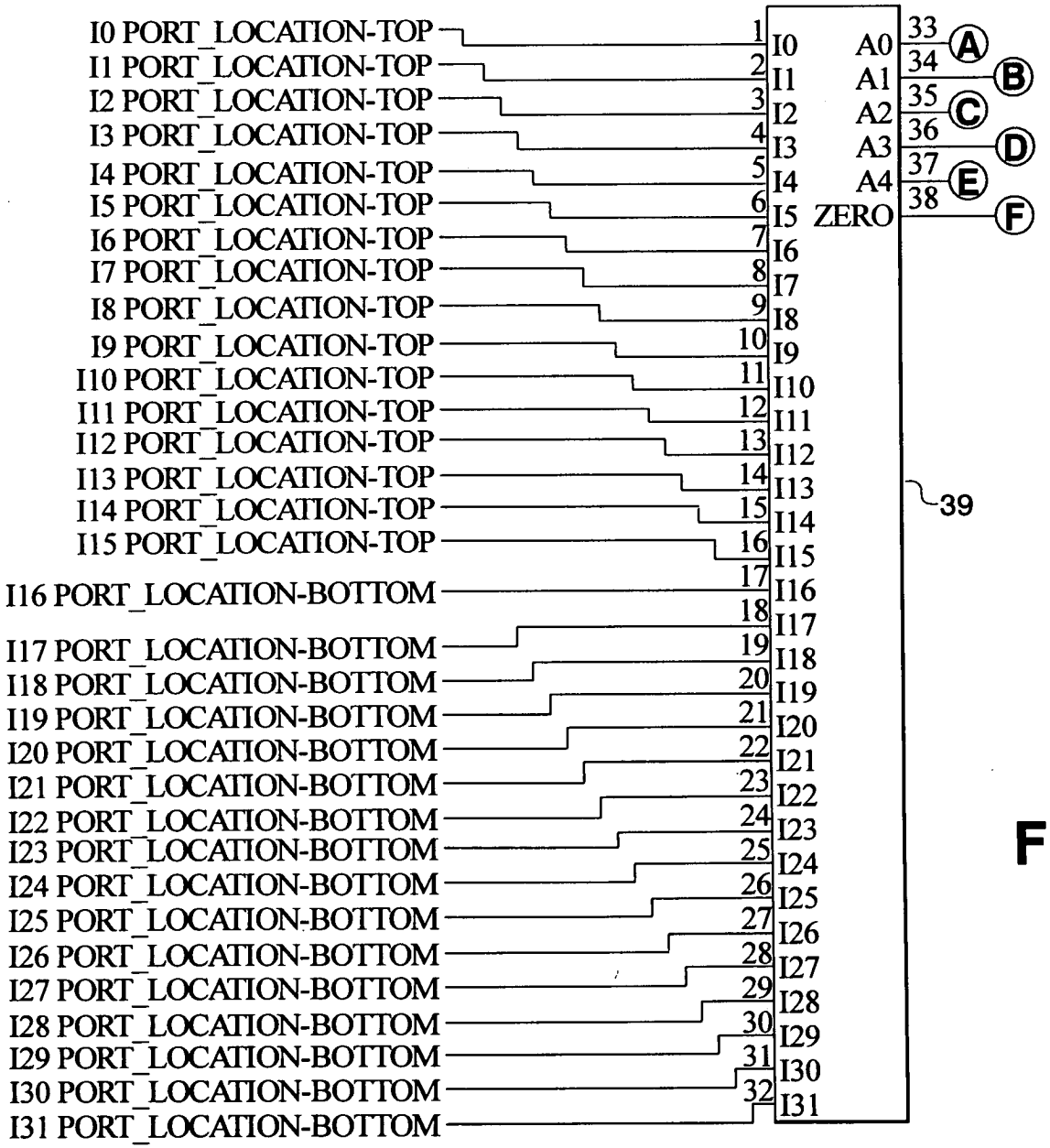

I0 PORT_LOCATION-TOP
I1 PORT_LOCATION-TOP
I2 PORT_LOCATION-TOP
I3 PORT_LOCATION-TOP
I4 PORT_LOCATION-TOP
I5 PORT_LOCATION-TOP
I6 PORT_LOCATION-TOP
I7 PORT_LOCATION-TOP
I8 PORT_LOCATION-TOP
I9 PORT_LOCATION-TOP
I10 PORT_LOCATION-TOP
I11 PORT_LOCATION-TOP
I12 PORT_LOCATION-TOP
I13 PORT_LOCATION-TOP
I14 PORT_LOCATION-TOP
I15 PORT_LOCATION-TOP
I16 PORT_LOCATION-BOTTOM
I17 PORT_LOCATION-BOTTOM
I18 PORT_LOCATION-BOTTOM
I19 PORT_LOCATION-BOTTOM
I20 PORT_LOCATION-BOTTOM
I21 PORT_LOCATION-BOTTOM
I22 PORT_LOCATION-BOTTOM
I23 PORT_LOCATION-BOTTOM
I24 PORT_LOCATION-BOTTOM
I25 PORT_LOCATION-BOTTOM
I26 PORT_LOCATION-BOTTOM
I27 PORT_LOCATION-BOTTOM
I28 PORT_LOCATION-BOTTOM
I29 PORT_LOCATION-BOTTOM
I30 PORT_LOCATION-BOTTOM
I31 PORT_LOCATION-BOTTOM
1 I0
2 I1
3 I2
4 I3
5 I4
6 I5
7 I6
8 I7
9 I8
10 I9
11 I10
12 I11
13 I12
14 I13
15 I14
16 I15
17 I16
18 I17
19 I18
20 I19
21 I20
22 I21
23 I22
24 I23
25 I24
26 I25
27 I26
28 I27
29 I28
30 I29
31 I30
32 I31
A0 33 A
A1 34 B
A2 35 C
A3 36 D
A4 37 E
ZERO 38 F
39

Figure 20(a)

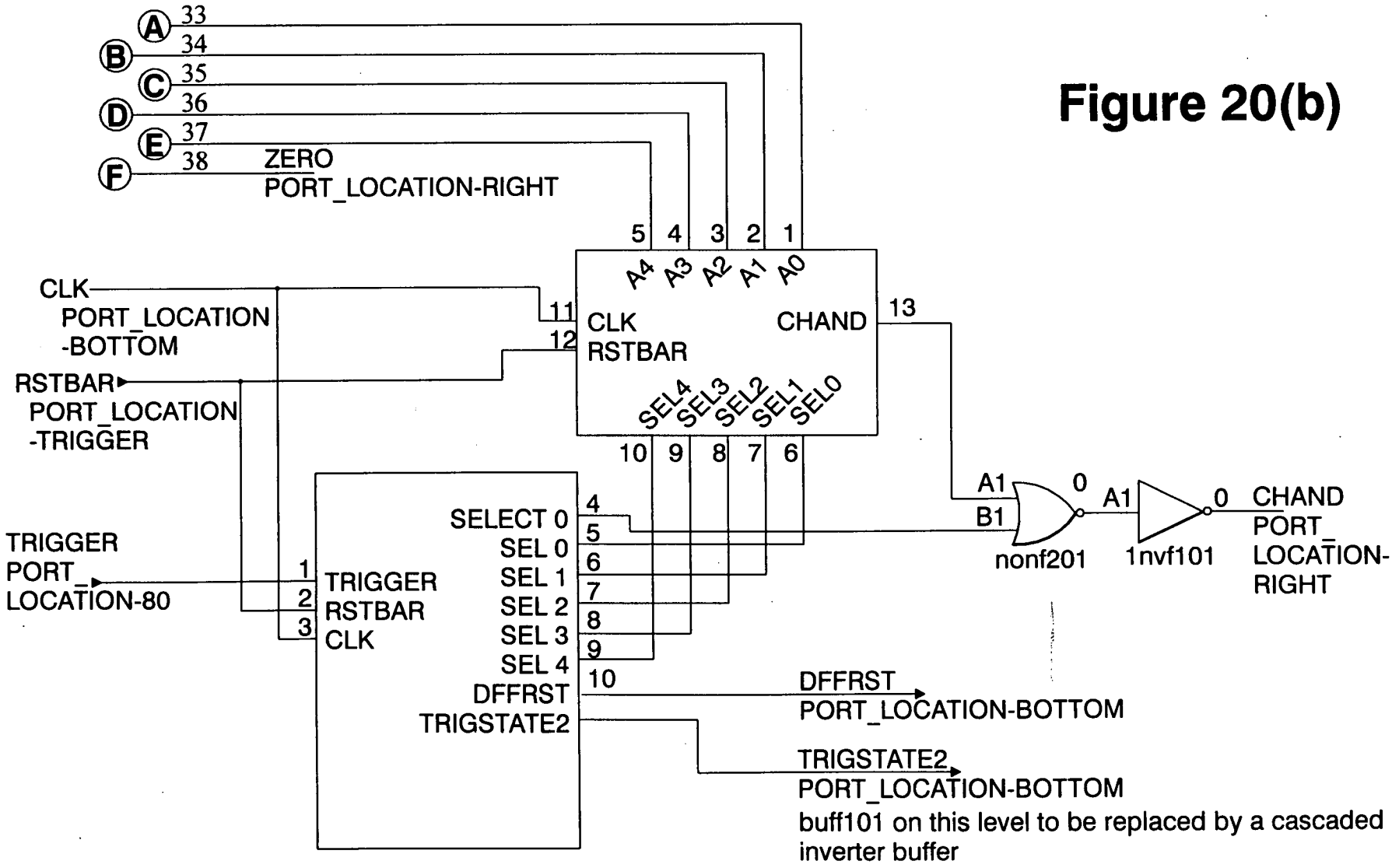

A
B
C
D
E
F
33
34
35
36
37
38
ZERO
PORT_LOCATION-RIGHT
5 4 3 2 1
A4 A3 A2 A1 A0
CLK
PORT_LOCATION
-BOTTOM
11
12
CLK
RSTBAR
CHAND
13
RSTBAR
PORT_LOCATION
-TRIGGER
SEL4 SEL3 SEL2 SEL1 SEL0
10 9 8 7 6
TRIGGER
PORT_
LOCATION-80
1
2
3
TRIGGER
RSTBAR
CLK
SELECT 0
SEL 0
SEL 1
SEL 2
SEL 3
SEL 4
DFFRST
TRIGSTATE2
4
5
6
7
8
9
10
A1
B1
0
nonf201
A1
0
1nvf101
CHAND
PORT_
LOCATION-
RIGHT
DFFRST
PORT_LOCATION-BOTTOM
TRIGSTATE2
PORT_LOCATION-BOTTOM
buff101 on this level to be replaced by a cascaded
inverter buffer

**Figure 20(b)**

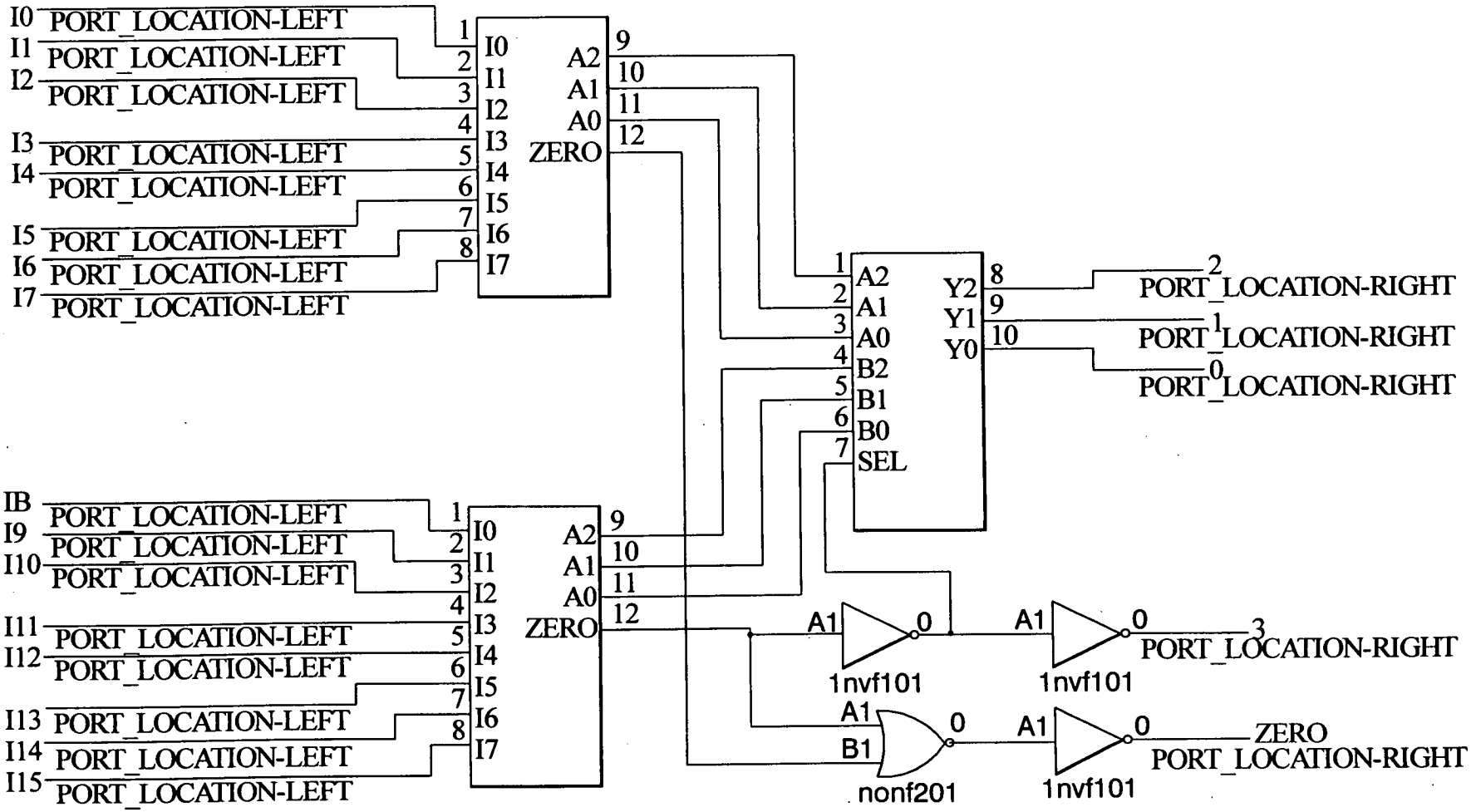

I0 PORT_LOCATION-LEFT
I1 PORT_LOCATION-LEFT
I2 PORT_LOCATION-LEFT
I3 PORT_LOCATION-LEFT
I4 PORT_LOCATION-LEFT
I5 PORT_LOCATION-LEFT
I6 PORT_LOCATION-LEFT
I7 PORT_LOCATION-LEFT
IB PORT_LOCATION-LEFT
I9 PORT_LOCATION-LEFT
I10 PORT_LOCATION-LEFT
I11 PORT_LOCATION-LEFT
I12 PORT_LOCATION-LEFT
I13 PORT_LOCATION-LEFT
I14 PORT_LOCATION-LEFT
I15 PORT_LOCATION-LEFT
A2
A1
A0
ZERO
B2
B1
B0
SEL
Y2
Y1
Y0
PORT_LOCATION-RIGHT
1nvf101
nonf201

**Figure 21**

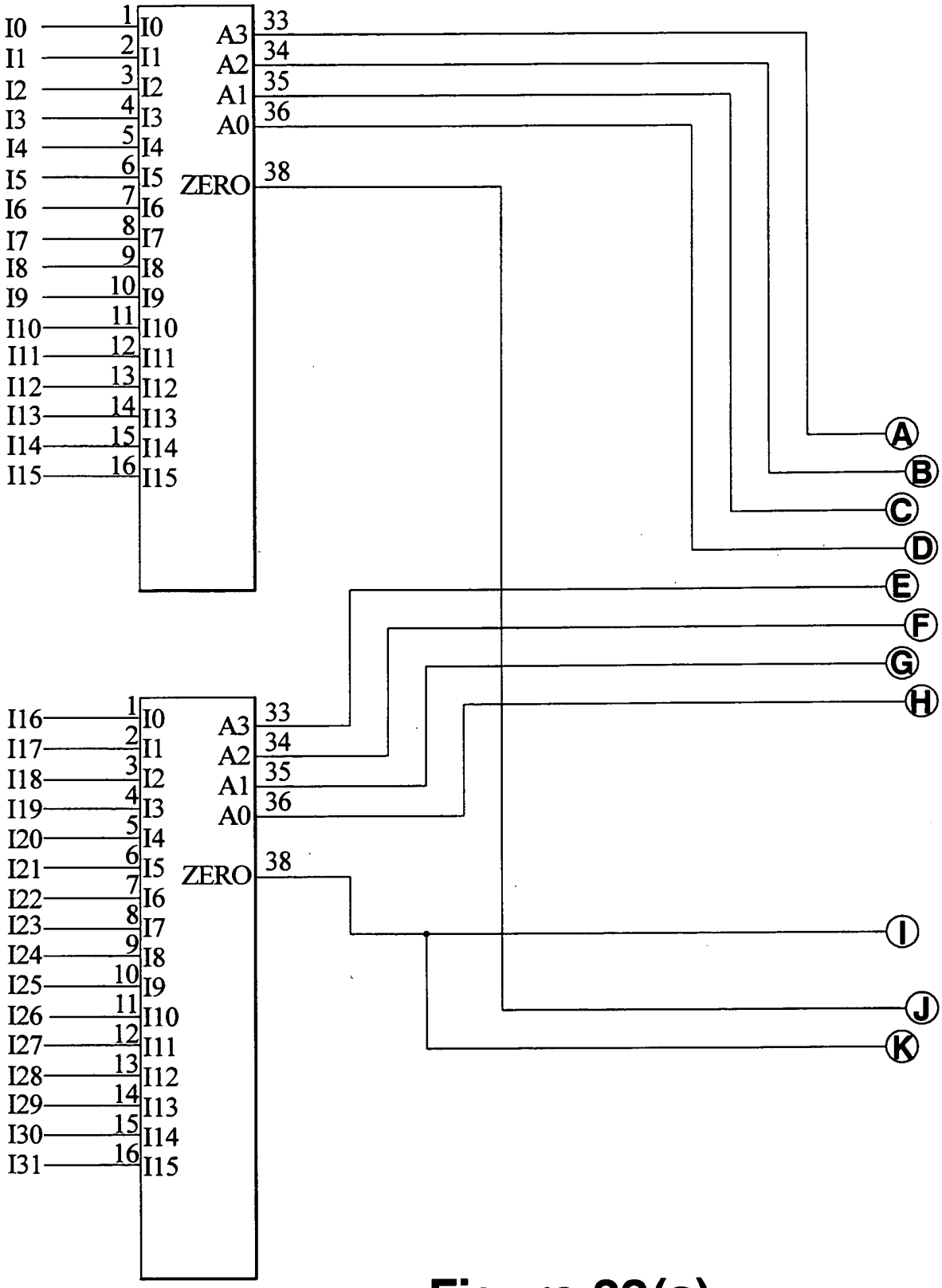

I0
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
I12
I13
I14
I15
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
I0
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
I12
I13
I14
I15
A3
A2
A1
A0
ZERO
33
34
35
36
38
A
B
C
D
E
F
G
H
I
J
K
I16
I17
I18
I19
I20
I21
I22
I23
I24
I25
I26
I27
I28
I29
I30
I31

**Figure 22(a)**

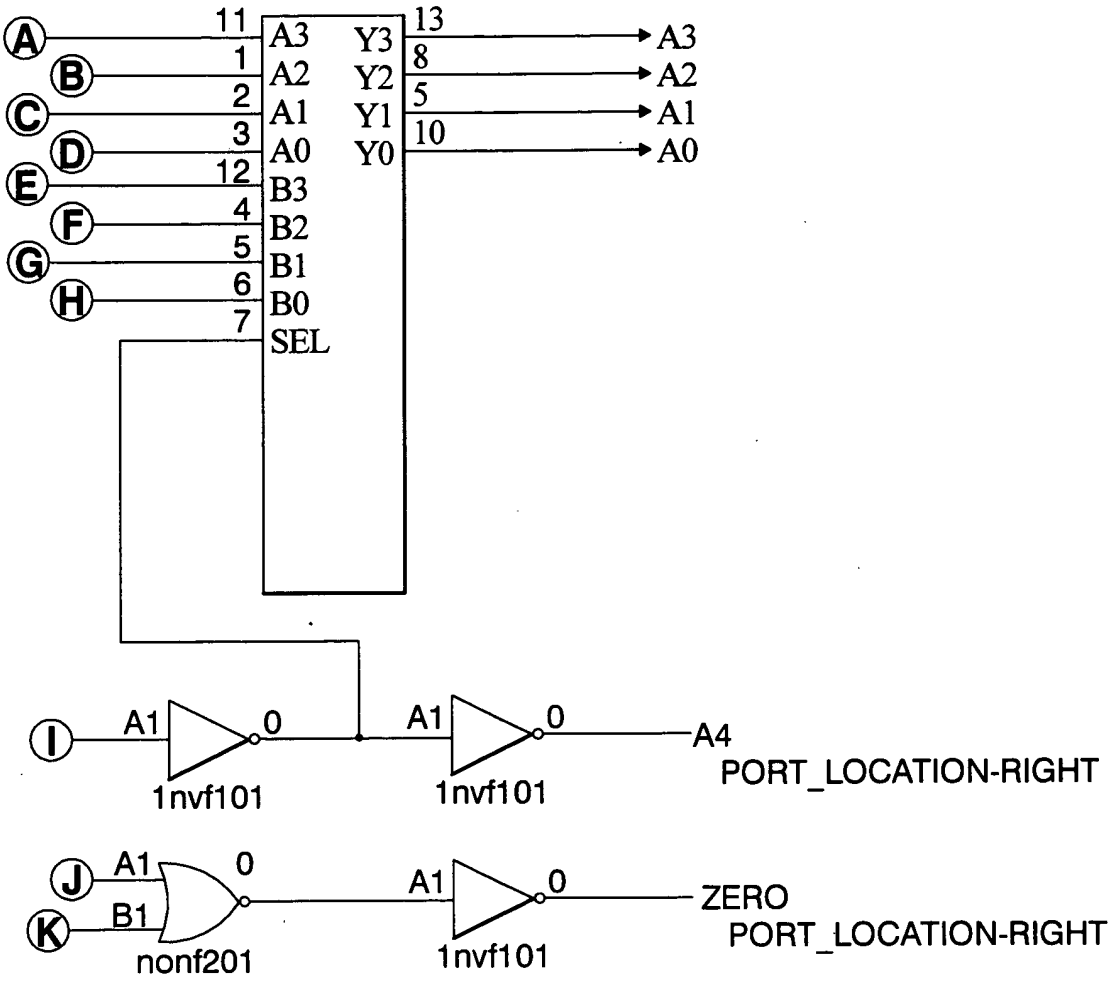

A
B
C
D
E
F
G
H
11
1
2
3
12
4
5
6
7
A3
A2
A1
A0
B3
B2
B1
B0
SEL
Y3
Y2
Y1
Y0
13
8
5
10
A3
A2
A1
A0
I
A1
0
1nvf101
A1
0
1nvf101
A4
PORT_LOCATION-RIGHT
J
K
A1
B1
0
nonf201
A1
0
1nvf101
ZERO
PORT_LOCATION-RIGHT

**Figure 22(b)**

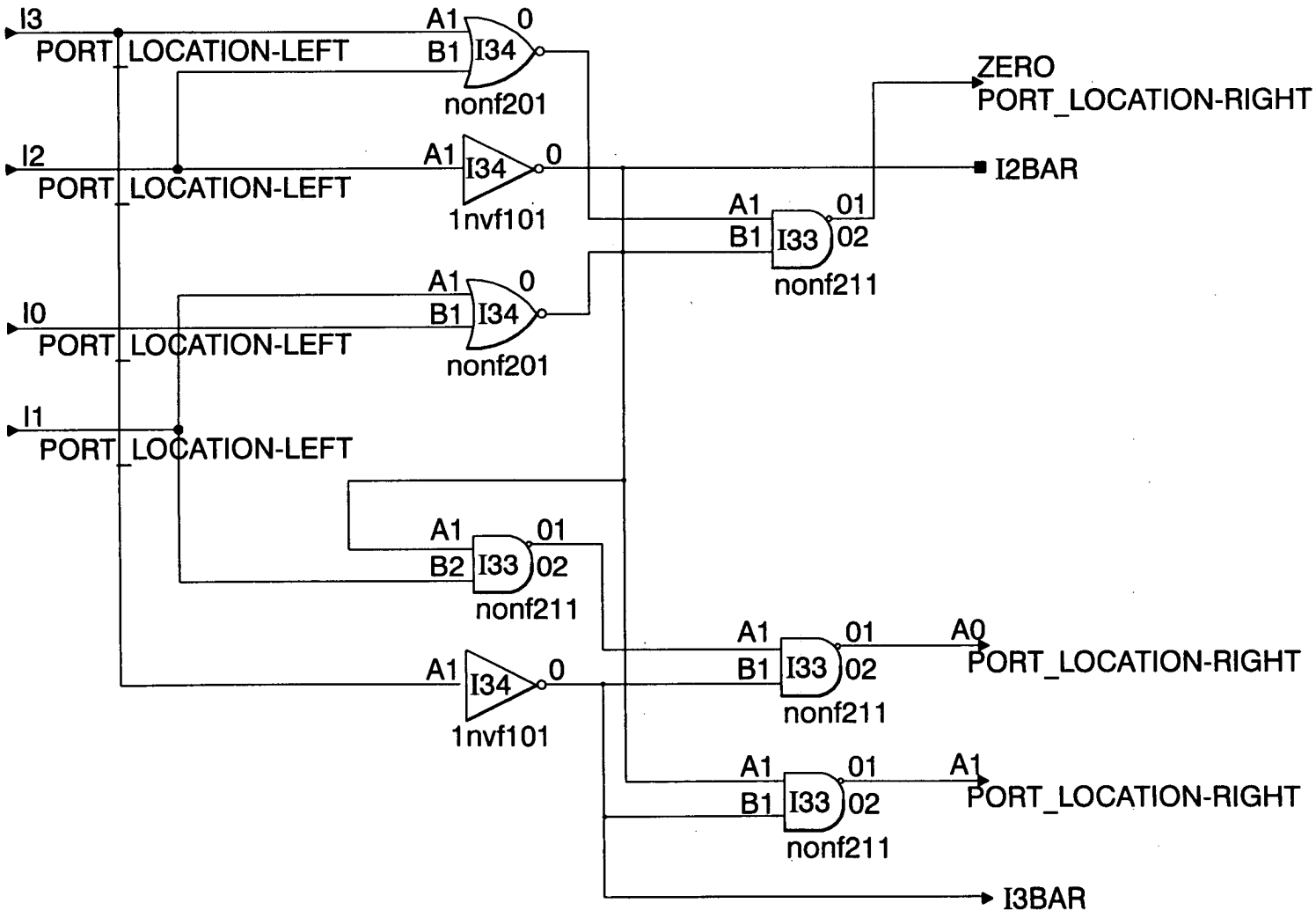

I3
PORT_LOCATION-LEFT
A1
B1
I34
0
nonf201
I2
PORT_LOCATION-LEFT
A1
I34
0
1nvf101
I0
PORT_LOCATION-LEFT
A1
B1
I34
0
nonf201
I1
PORT_LOCATION-LEFT
A1
B2
I33
01
02
nonf211
A1
I34
0
1nvf101
A1
B1
I33
01
02
nonf211
ZERO
PORT_LOCATION-RIGHT
I2BAR
A1
B1
I33
01
02
nonf211
A0
PORT_LOCATION-RIGHT
A1
B1
I33
01
02
nonf211
A1
PORT_LOCATION-RIGHT
I3BAR

**Figure 23**

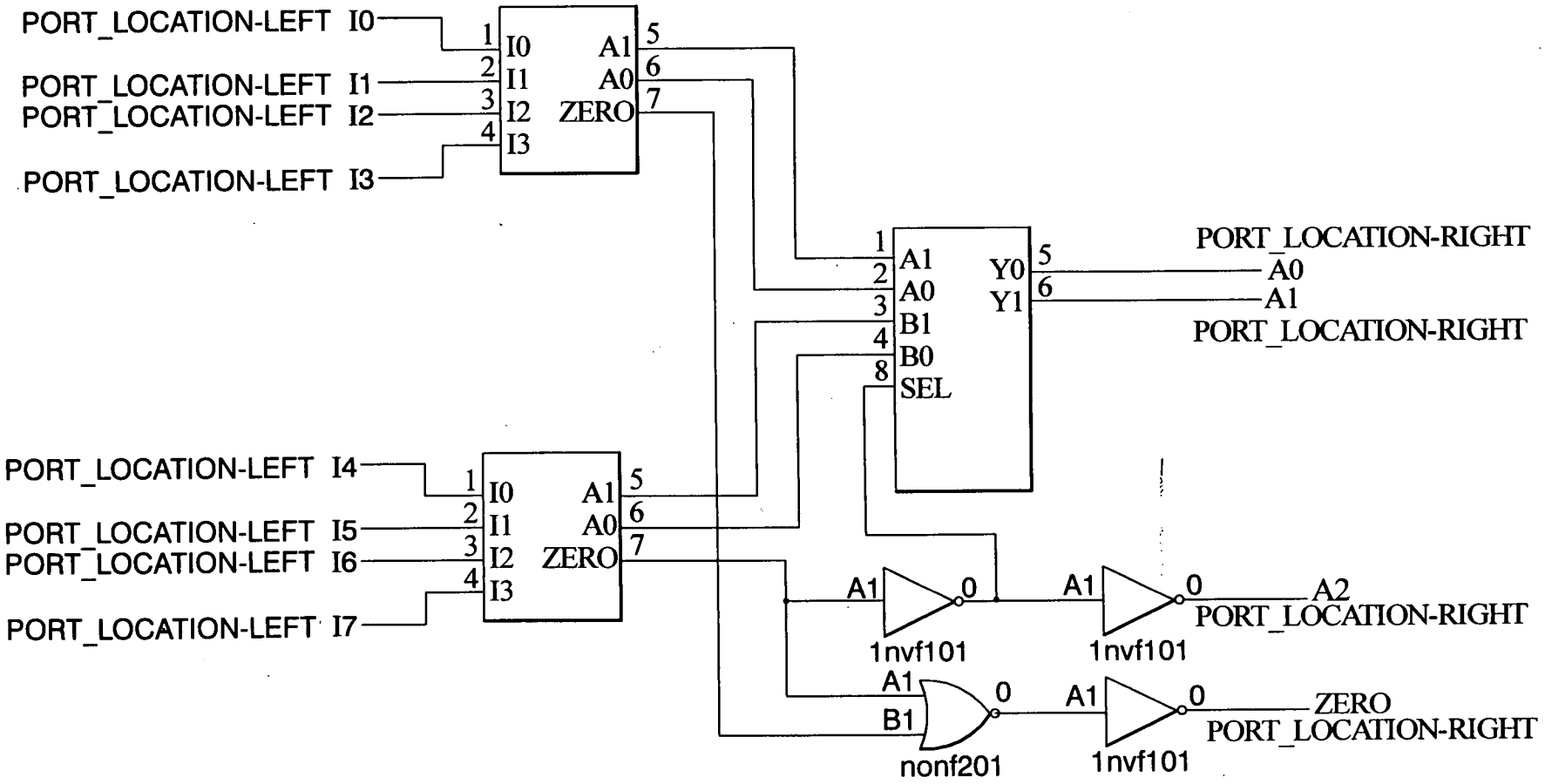
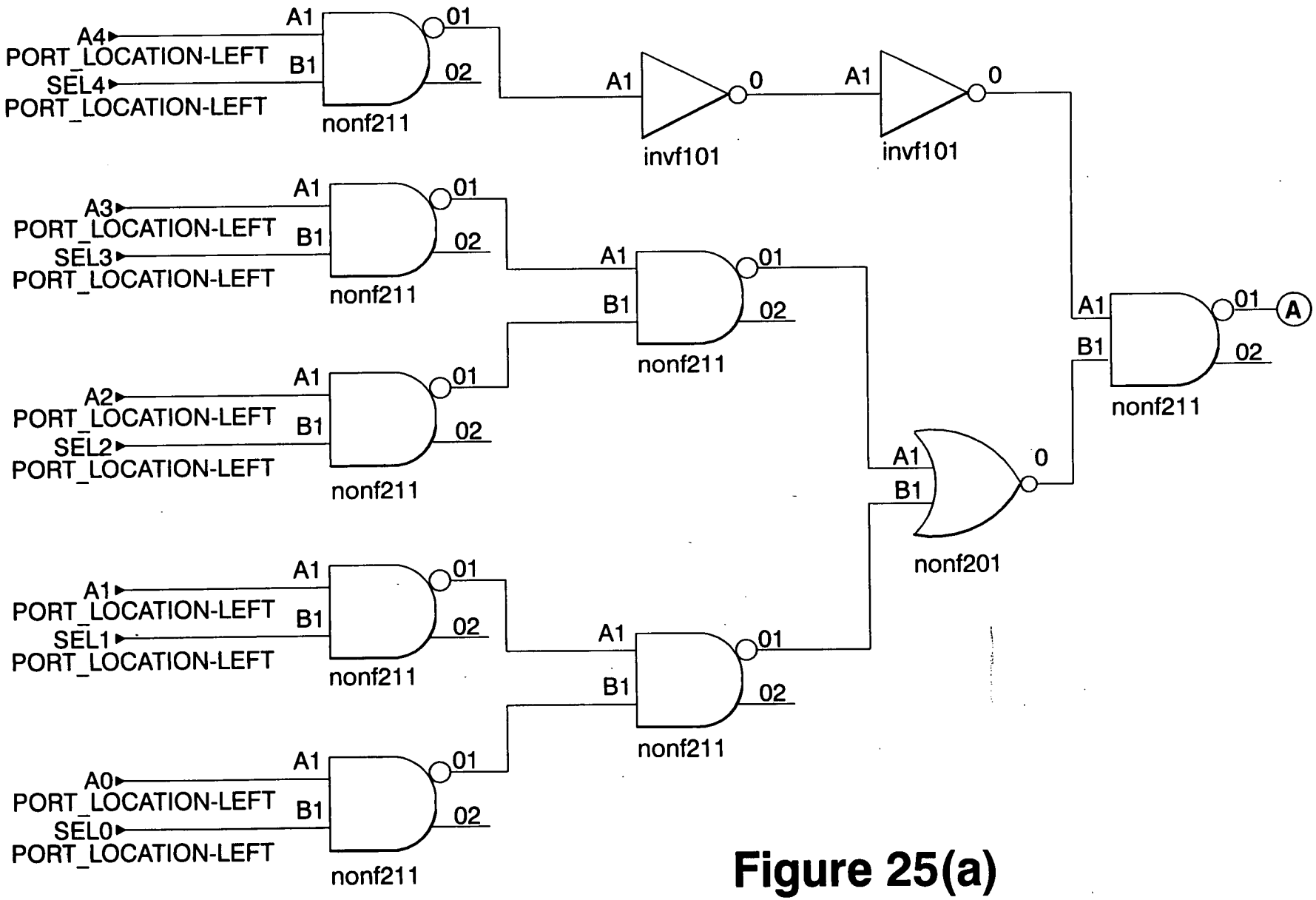

PORT_LOCATION-LEFT I0
PORT_LOCATION-LEFT I1
PORT_LOCATION-LEFT I2
PORT_LOCATION-LEFT I3
1
2
3
4
I0
I1
I2
I3
A1
A0
ZERO
5
6
7
PORT_LOCATION-LEFT I4
PORT_LOCATION-LEFT I5
PORT_LOCATION-LEFT I6
PORT_LOCATION-LEFT I7
1
2
3
4
I0
I1
I2
I3
A1
A0
ZERO
5
6
7
1
2
3
4
8
A1
A0
B1
B0
SEL
Y0
Y1
5
6
PORT_LOCATION-RIGHT
A0
A1
PORT_LOCATION-RIGHT
A1
0
1nvf101
A1
0
A2
PORT_LOCATION-RIGHT
1nvf101
A1
B1
0
nonf201
A1
0
ZERO
PORT_LOCATION-RIGHT
1nvf101

**Figure 24**


A4
PORT_LOCATION-LEFT
SEL4
PORT_LOCATION-LEFT
A1
B1
01
02
nonf211
A1
0
invf101
A1
0
invf101
A3
PORT_LOCATION-LEFT
SEL3
PORT_LOCATION-LEFT
nonf211
A2
PORT_LOCATION-LEFT
SEL2
PORT_LOCATION-LEFT
nonf211
A1
PORT_LOCATION-LEFT
SEL1
PORT_LOCATION-LEFT
nonf211
A0
PORT_LOCATION-LEFT
SEL0
PORT_LOCATION-LEFT
nonf211
nonf211
nonf211
nonf201
nonf211
A
Figure 25(a)

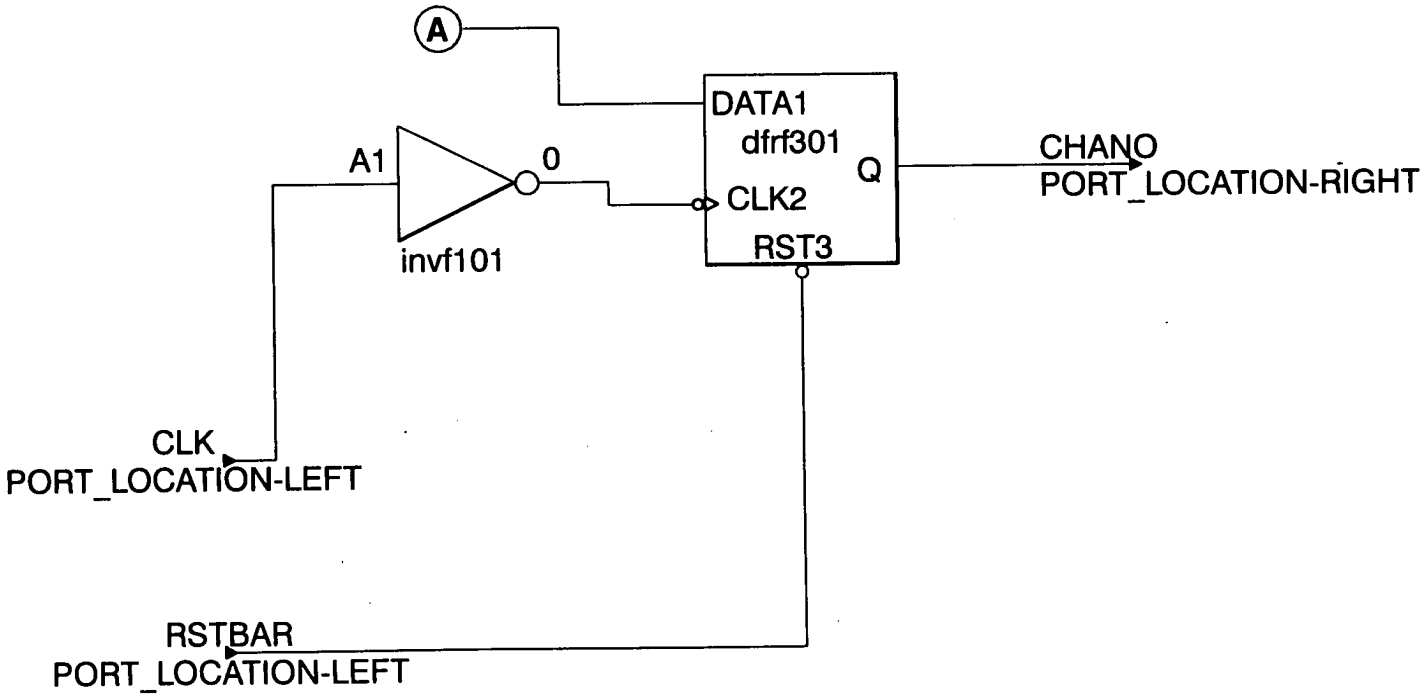

A
DATA1
dfrf301
Q
CHANO
PORT_LOCATION-RIGHT
A1
0
CLK2
RST3
invf101
CLK
PORT_LOCATION-LEFT
RSTBAR
PORT_LOCATION-LEFT

**Figure 25(b)**

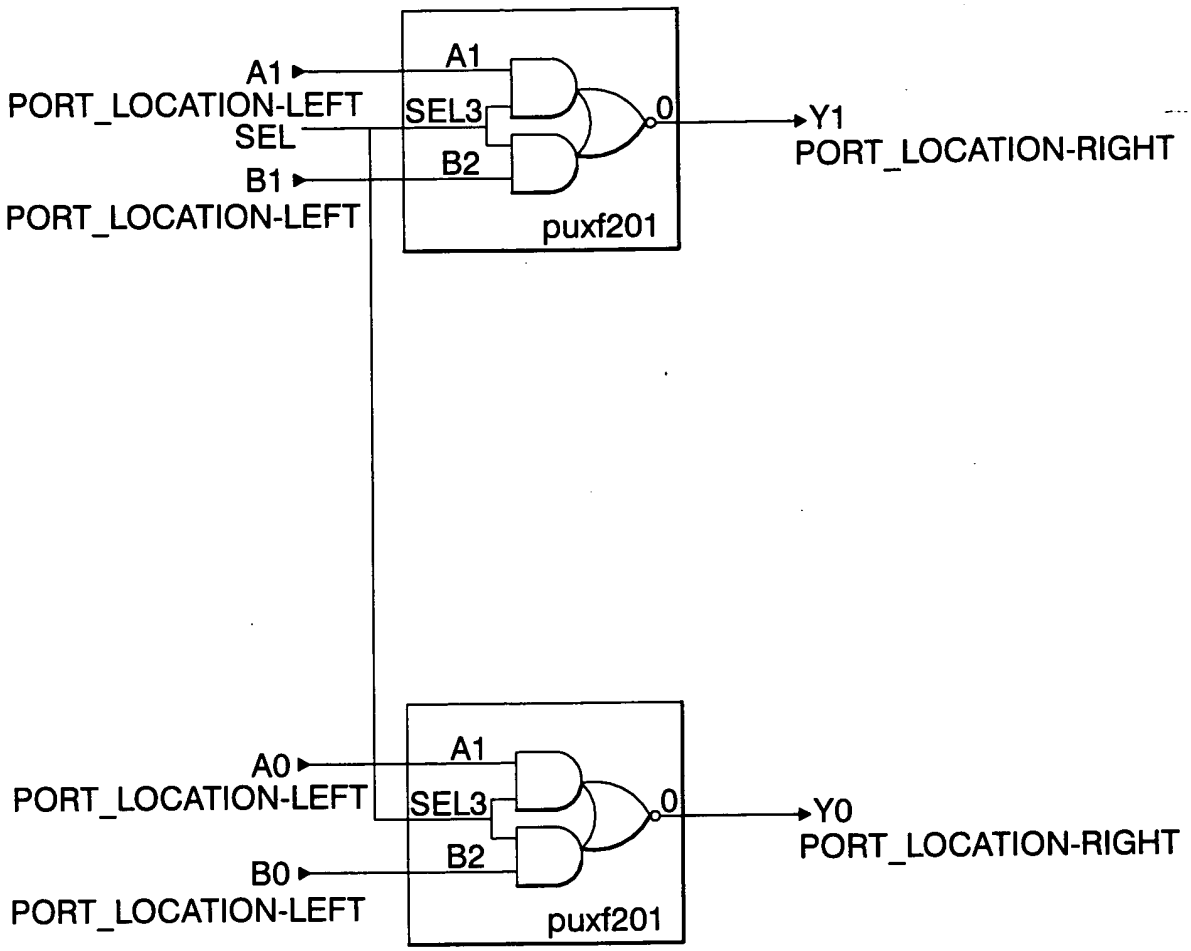

A1
PORT_LOCATION-LEFT
SEL
B1
PORT_LOCATION-LEFT
A1
SEL3
B2
0
puxf201
Y1
PORT_LOCATION-RIGHT
A0
PORT_LOCATION-LEFT
B0
PORT_LOCATION-LEFT
A1
SEL3
B2
0
puxf201
Y0
PORT_LOCATION-RIGHT

**Figure 26**

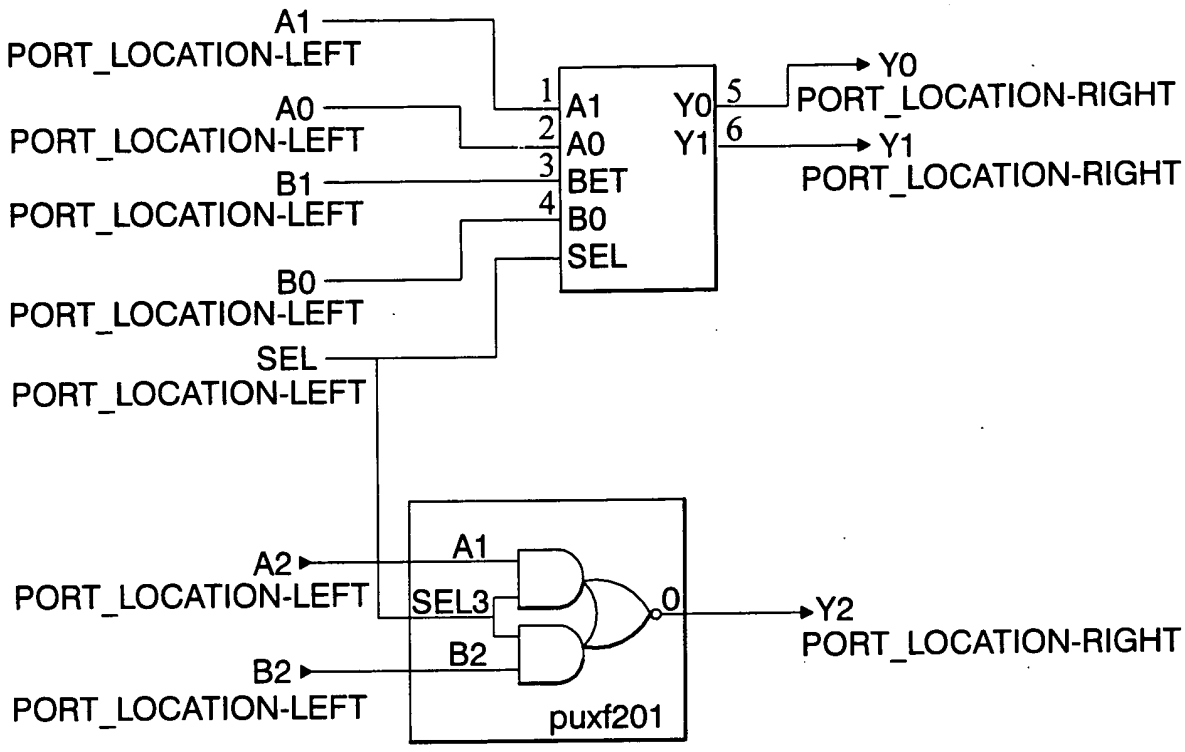

A1
PORT_LOCATION-LEFT
A0
PORT_LOCATION-LEFT
B1
PORT_LOCATION-LEFT
B0
PORT_LOCATION-LEFT
SEL
PORT_LOCATION-LEFT
1
2
3
4
A1
A0
BET
B0
SEL
Y0
Y1
5
6
Y0
PORT_LOCATION-RIGHT
Y1
PORT_LOCATION-RIGHT
A2
PORT_LOCATION-LEFT
B2
PORT_LOCATION-LEFT
A1
SEL3
B2
0
puxf201
Y2
PORT_LOCATION-RIGHT

**Figure 27**

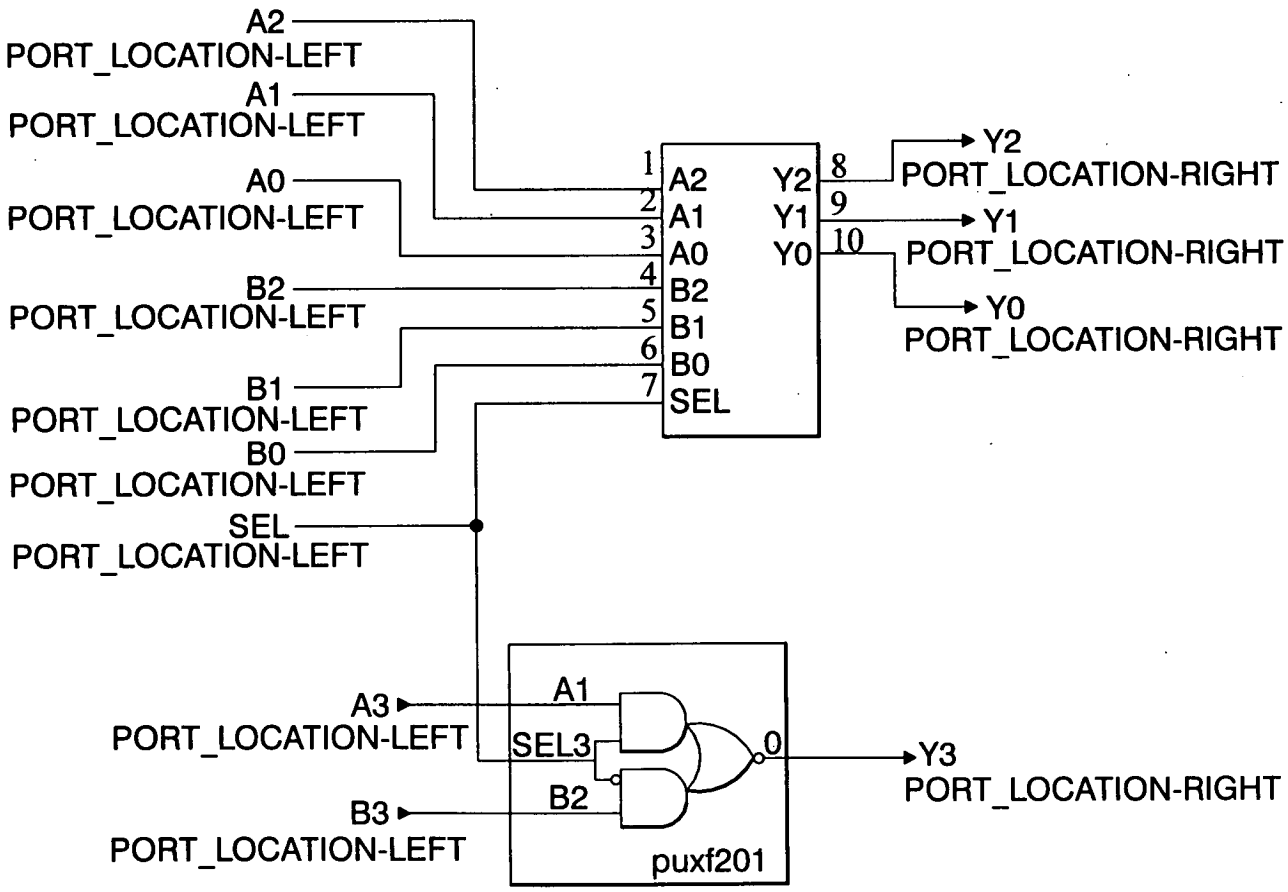

A2
PORT_LOCATION-LEFT
A1
PORT_LOCATION-LEFT
A0
PORT_LOCATION-LEFT
B2
PORT_LOCATION-LEFT
B1
PORT_LOCATION-LEFT
B0
PORT_LOCATION-LEFT
SEL
PORT_LOCATION-LEFT
1 A2
2 A1
3 A0
4 B2
5 B1
6 B0
7 SEL
Y2 8
Y1 9
Y0 10
Y2
PORT_LOCATION-RIGHT
Y1
PORT_LOCATION-RIGHT
Y0
PORT_LOCATION-RIGHT
A3
PORT_LOCATION-LEFT
B3
PORT_LOCATION-LEFT
A1
SEL3
B2
0
puxf201
Y3
PORT_LOCATION-RIGHT

**Figure 28**

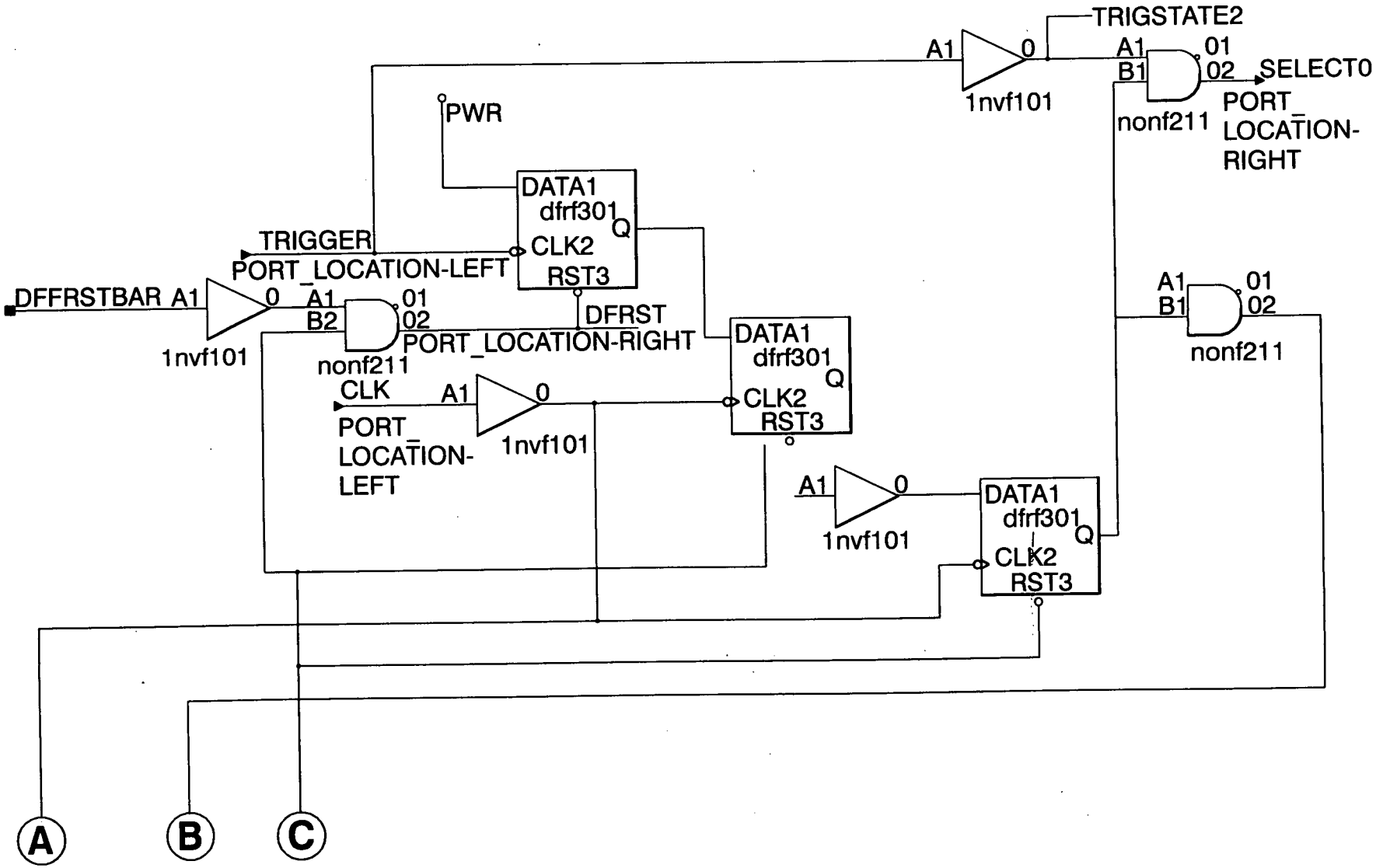

TRIGSTATE2
A1
0
1nvf101
A1
B1
01
02
SELECT0
nonf211
PORT_
LOCATION-
RIGHT
PWR
DATA1
dfrf301
Q
CLK2
RST3
TRIGGER
PORT_LOCATION-LEFT
DFFRSTBAR A1
0
A1
B2
01
02
DFRST
PORT_LOCATION-RIGHT
1nvf101
nonf211
A1
B1
01
02
nonf211
CLK
A1
0
PORT_
LOCATION-
LEFT
1nvf101
DATA1
dfrf301
Q
CLK2
RST3
A1
0
1nvf101
DATA1
dfrf301
Q
CLK2
RST3
A
B
C

**Figure 29(a)**

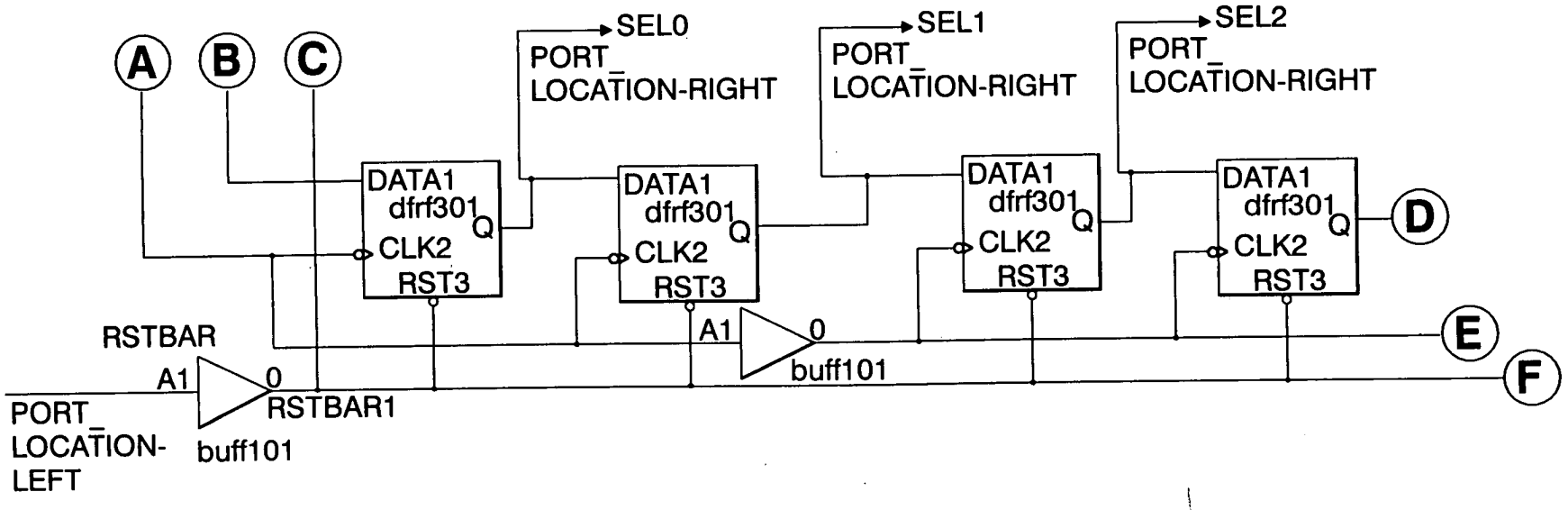

A
B
C
SEL0
PORT_
LOCATION-RIGHT
SEL1
PORT_
LOCATION-RIGHT
SEL2
PORT_
LOCATION-RIGHT
DATA1
dfrf301
Q
CLK2
RST3
D
E
F
RSTBAR
A1
0
RSTBAR1
buff101
PORT_
LOCATION-
LEFT

**Figure 29(b)**

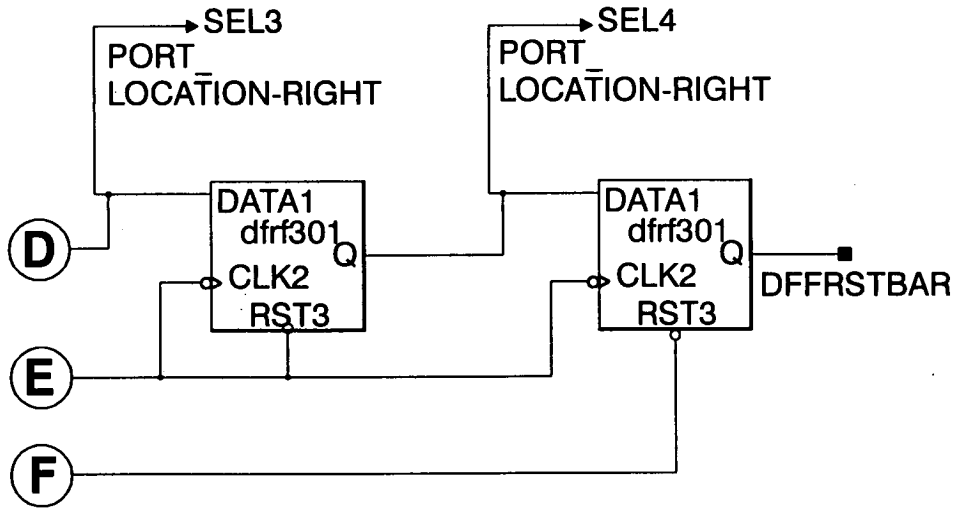

SEL3
PORT_
LOCATION-RIGHT
SEL4
PORT_
LOCATION-RIGHT
DATA1
dfrf301
Q
CLK2
RST3
DATA1
dfrf301
Q
CLK2
RST3
DFFRSTBAR
D
E
F

**Figure 29(c)**

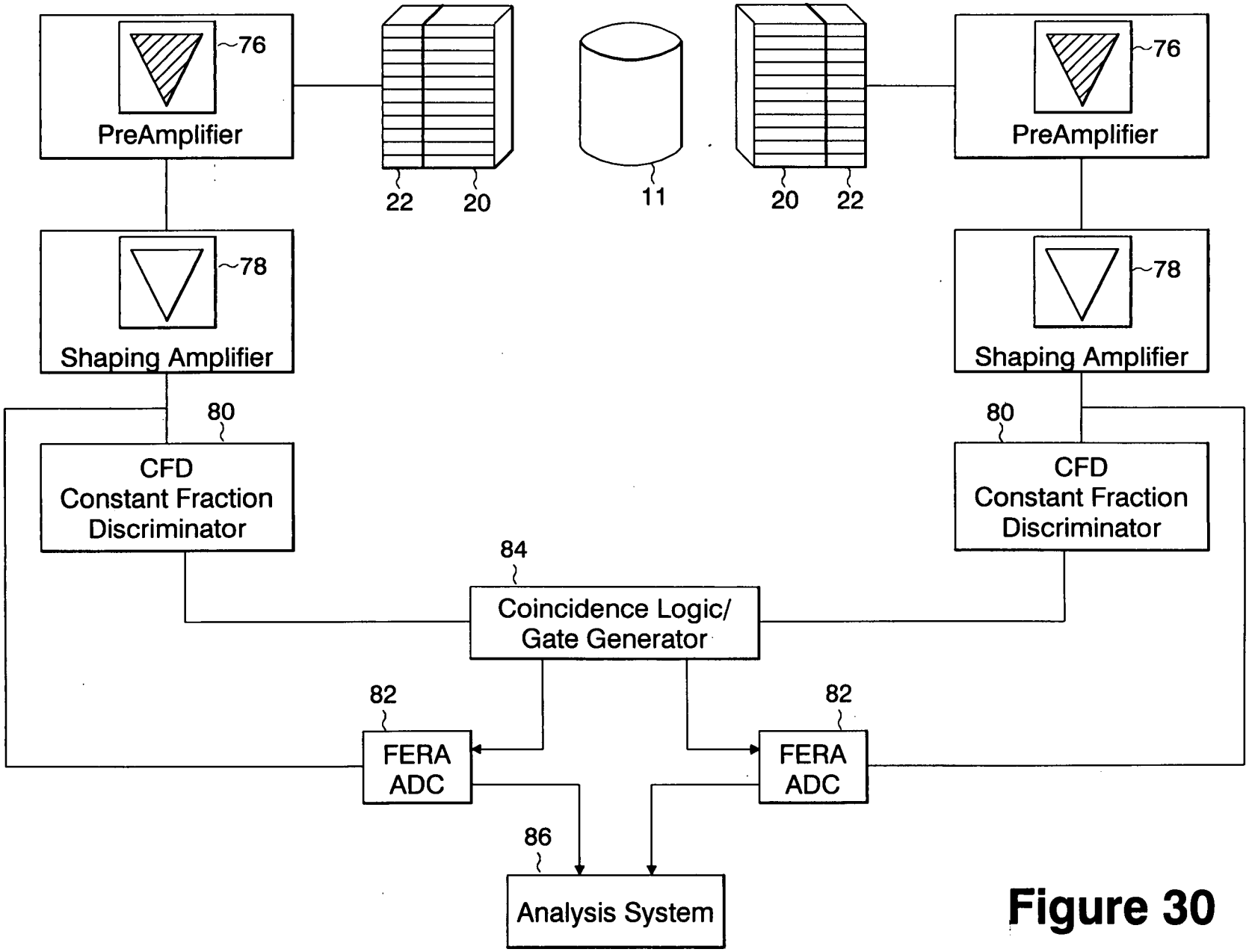

76
PreAmplifier
22
20
11
20
22
76
PreAmplifier
78
Shaping Amplifier
78
Shaping Amplifier
80
CFD
Constant Fraction
Discriminator
80
CFD
Constant Fraction
Discriminator
84
Coincidence Logic/
Gate Generator
82
FERA
ADC
82
FERA
ADC
86
Analysis System

Figure 30

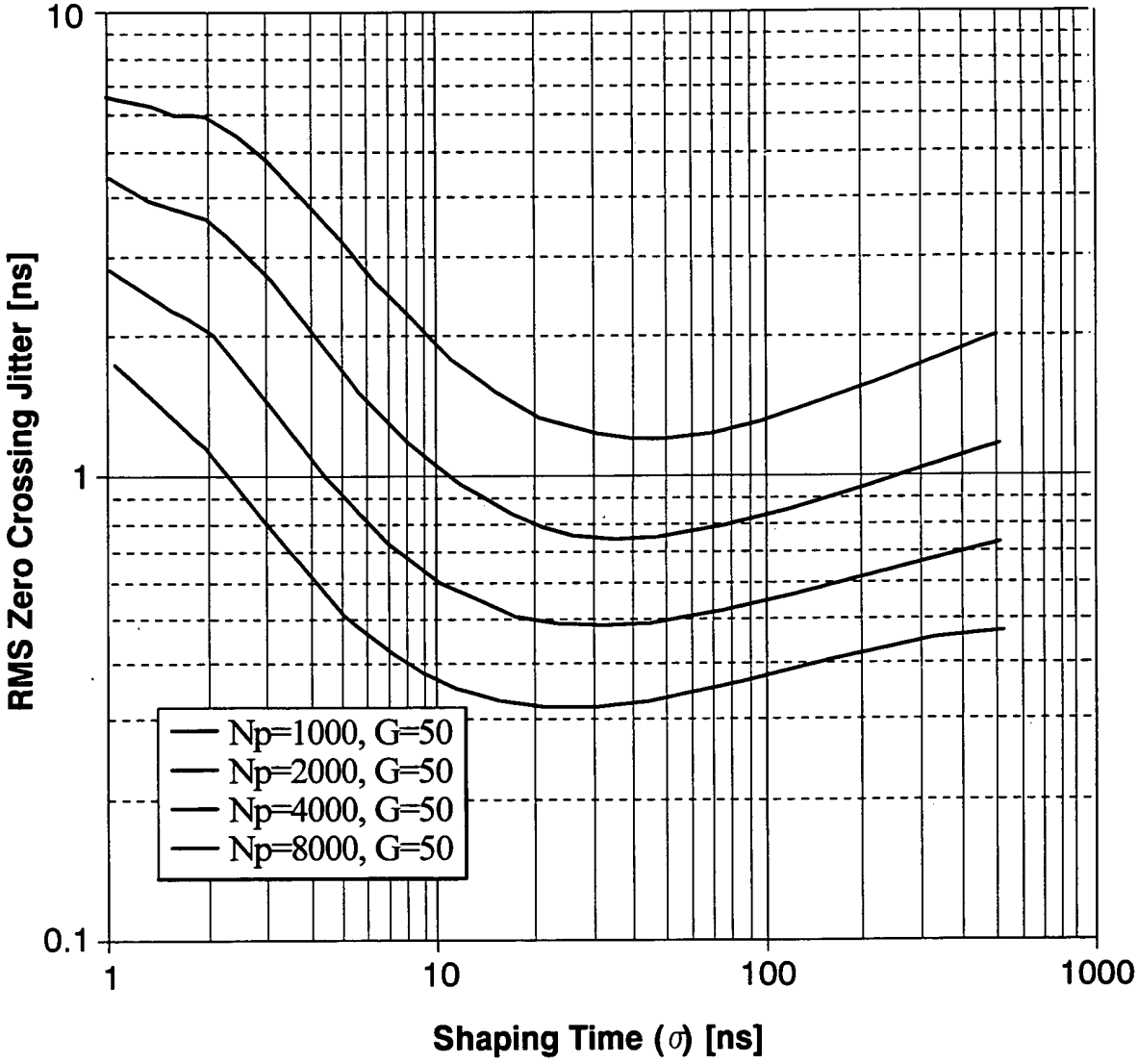

10
1
0.1
RMS Zero Crossing Jitter [ns]
1
10
100
1000
Shaping Time (σ) [ns]
Np=1000, G=50
Np=2000, G=50
Np=4000, G=50
Np=8000, G=50

**Figure 31**

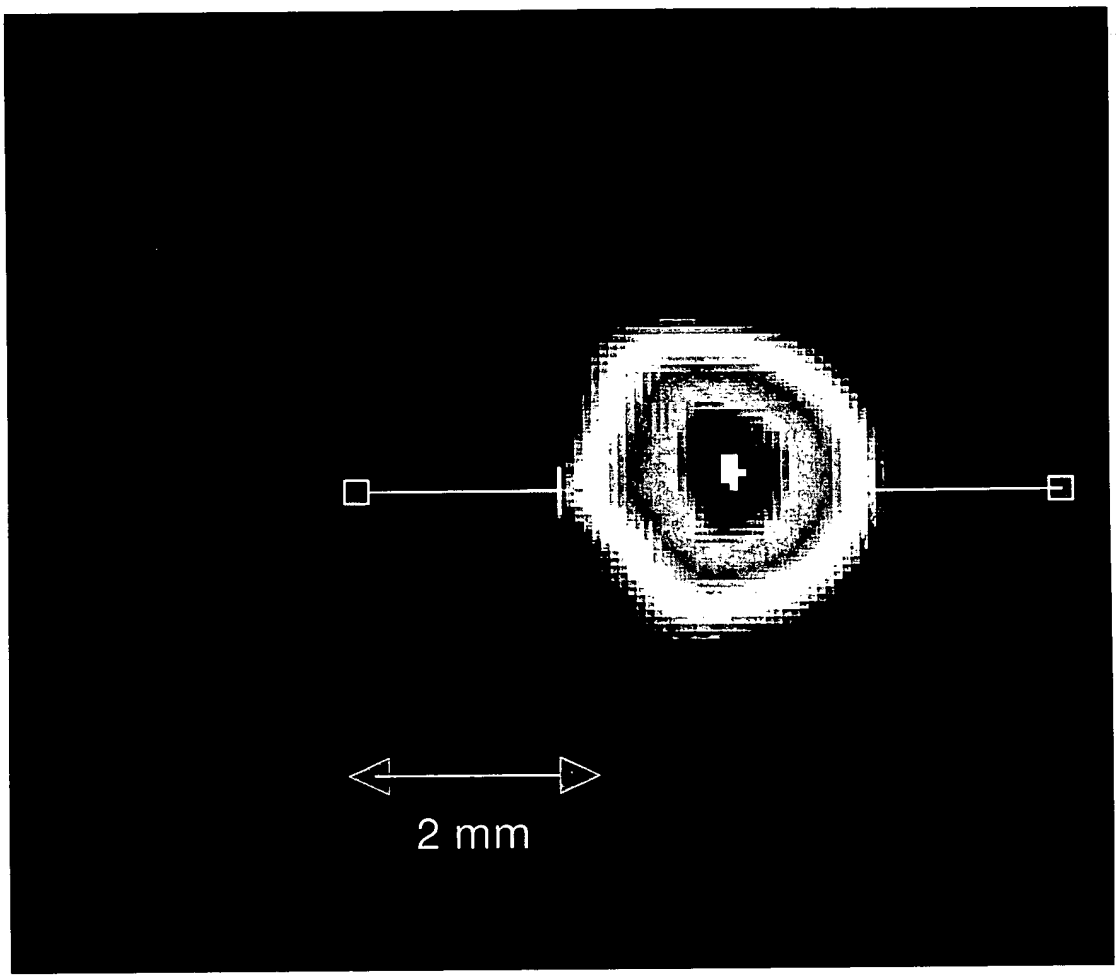



**Figure 32a**

BEST AVAILABLE COPY

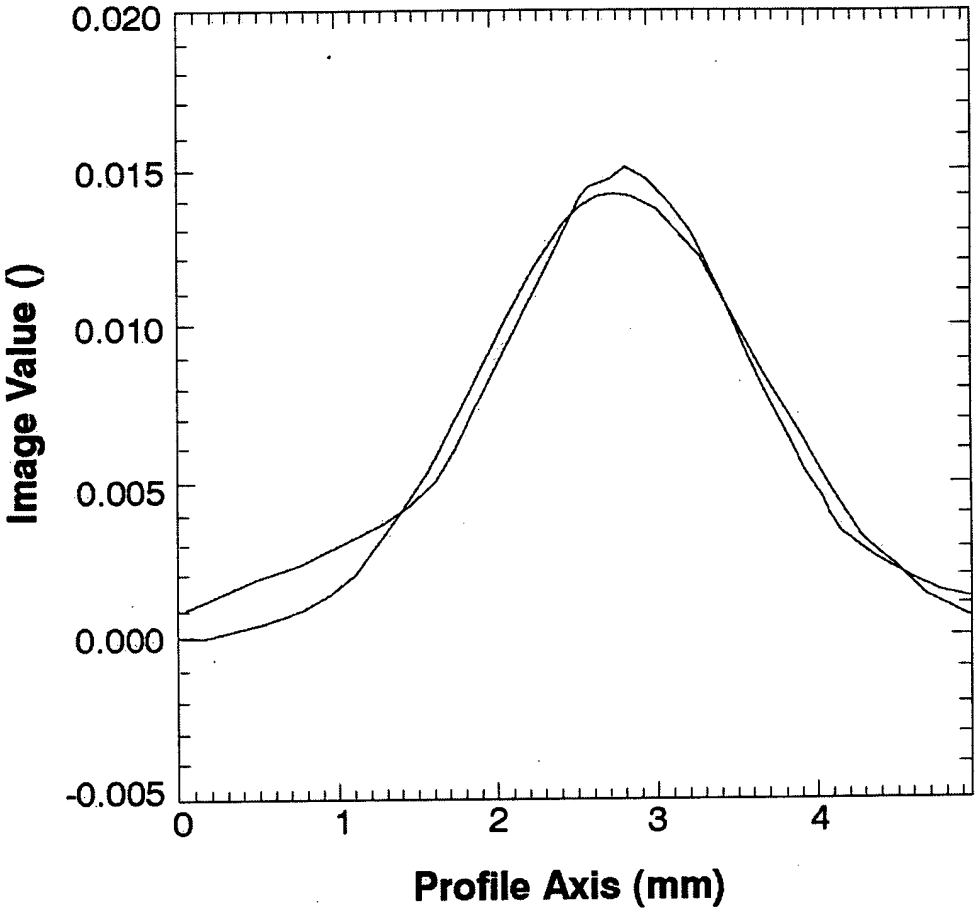

0.020
0.015
0.010
0.005
0.000
-0.005
Image Value ()
0
1
2
3
4
Profile Axis (mm)

Figure 32b

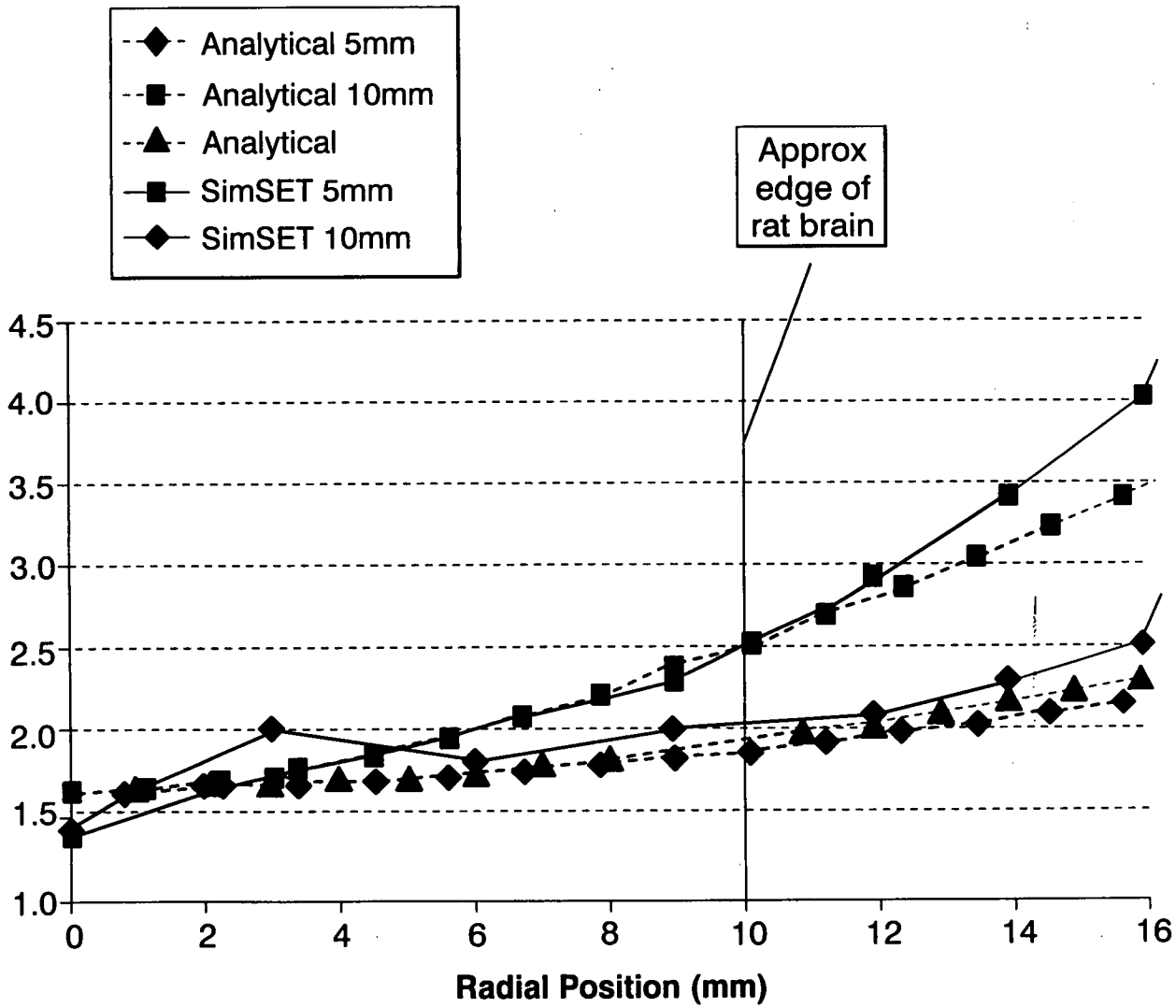

Analytical 5mm
Analytical 10mm
Analytical
SimSET 5mm
SimSET 10mm
Approx edge of rat brain
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0
2
4
6
8
10
12
14
16
Radial Position (mm)

**Figure 33**

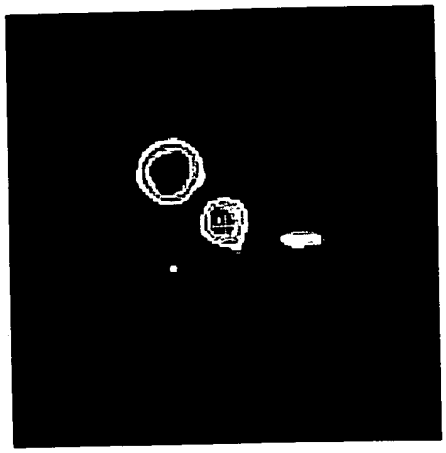


Figure 34a

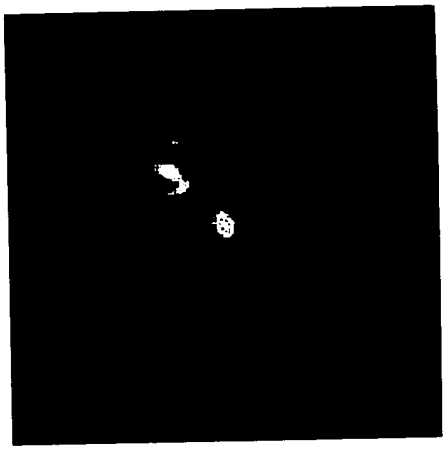


Figure 34b

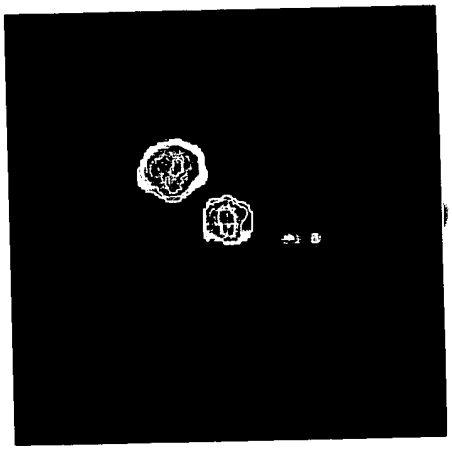


Figure 34c

BEST AVAILABLE COPY